Doctoral Thesis

A Study of BTI-Induced Variability and Highly Sensitive On-Chip Digital Aging Monitor for High Reliability

2021

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Abstract

This thesis reports the study of bias temperature instability (BTI) induced variability by measuring ring-oscillators (ROs) in advanced Complementary Metal-Oxide Semiconductor (CMOS) process technologies for optimal robust design. Two variability of BTI are discussed, one is layout dependent variability and the other is statistical BTI variability in a chip. In addition, RO-based on-chip monitors with highly sensitive BTI and hot carrier injection (HCI) are described for high reliability and optimal guard-band.

First, the background of this research area and purpose of this study are explained. The challenges of design for reliability of integrated circuit (IC) are increasing with the spread of application, demand of high performance and low power, and progress of process scaling. Therefore, the importance of study of BTI induced variability and on-chip aging monitor is increased for satisfying both high performance and high reliability. The characteristics of BTI and HCI and those impact on logic circuit are briefly described for better understanding of this study.

In the second chapter, an analysis methodology of the impact of Local Layout Effect (LLE) of BTI on logic circuits by measuring Ring-Oscillators (RO) is described. The basic concept of the analysis methodology is based on the difference of sensitivity of BTI on delay in each standard cell type. The impact of BTI's LLE on various standard cells is analyzed by comparing estimated delay degradation without considering LLE and measured delay degradation. The measurement result of test chip fabricated in 10 nm Fin Field Effect Transistor (FinFET) is demonstrated. The impact of BTI's LLE on logic circuit design is also discussed.

The third chapter describes an analysis of local variability of BTI by measuring RO on various processes and its impact on logic circuit and SRAM. The evaluation results based on measuring ROs of test chips fabricated in a 7 nm FinFET process, 16/14 nm generation FinFET processes and a 28 nm planar process reveal that the standard deviations of threshold voltage (V_{th}) degradation ($\sigma(\Delta V_{thp})$) caused by Negative BTI (NBTI) are proportional to the square root of the mean value ($\mu(\Delta V_{thp})$) at any stress time, V_{th} flavors and various recovery conditions. While the amount of local BTI variation depends on the gate length, width and number of fins, the amount of local BTI variation at the 7 nm FinFET process becomes larger than other processes. Based on these measurement results, an analysis result of its impact on logic circuits and a static random access memory (SRAM) are demonstrated.

In the forth chapter, on-chip NBTI, positive BTI (PBTI) and HCI monitors are presented. These monitors are composed of standard cell based unbalanced ROs. In case of a NBTI sensitive

RO (NBTI-RO) and a PBTI sensitive RO (PBTI-RO), these are consisted with unbalanced drive strength combination of NAND and NOR cells, realizing over 4 times high sensitivity at DC stress compared with a normal Inverter (INV) based RO. This high sensitivity is due to the unbalanced delay and increase of ΔV_{th} sensitivity on delay by stacked MOS FETs. The Miller effect caused by large drive strength cell mitigates PBTI and NBTI influence on NBTI-RO and PBTI-RO, respectively. In addition, R-NBTI-RO, whose cell connection order is opposite to NBTI-RO, is used for further increase and decrease of NBTI and PBTI sensitivity for NBTI monitor, respectively. As a result, 6.2x NBTI sensitivity compared with normal INV-RO and negligibly small PBTI sensitivity are achieved in the 7 nm FinFET process. In HCI monitor, HCI degradation is 3.6x emphasized by using unbalanced drive strength configuration of INV cell by simulating worst-case waveform of logic circuit. The measurement results of test chips fabricated in the 28 nm HKMG process and the 7 nm FinFET process are demonstrated.

In the last chapter, the conclusion of this study is described.

Contents

Chapter 1 Introduction

1.1. Background of Research Area

The Large-Scale Integration (LSI) circuits are widely used in current information society. In LSIs, Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are widely used. As process scaling of MOSFET proceeds, the performance and transistor density of LSIs are increased with decreasing power consumption and cost of the transistor [1]. As a result, the application of LSIs has expanded, including not only consumer electronics such as personal computer and mobile phone, but also data center, infrastructure equipment, industrial instruments, automobiles, medical instruments and so on. With the expansion of applications of LSIs, the reliability of semiconductor devices becomes more and more important because the failure of LSIs has a big impact on information society.

In recent years, it is inevitable to pursue higher performance for automotive LSIs such as advanced driver-assistance systems (ADAS) and autonomous driving [2][3]. Higher performance should be achieved under limited power budget at high temperature condition of cars because huge power consumption leads to requirement of huge and expensive cooling systems in the car's Electronic Control Unit (ECU). which is one of the key motivations for automotive chips to apply advanced process technologies such as a 7 nm Fin Field Effect Transistor (FinFET) process [4][5]. A high reliability is also required in automotive chips especially for autonomous driving era because car accidents directly threaten human life. On the other hand, the reliability of semiconductor devices becomes more severe as process technology proceeds.

The aging degradation of MOSFETs such as bias temperature instabilities (BTI) and Hot Carrier Injection (HCI) are one of the major reliability concerns and the high temperature condition of cars causes a big impact on both power consumption and reliability. As operation temperature increases, aging degradation is increased. Furthermore, it is expected that the paradigm shift of car usage by autonomous driving would worsen reliability due to increase annual mileage of cars. In general, chip designers take guard-band (GB) into account in product design and test [6] to prevent delay failures caused by device aging effects at the end of the product lifetime. Figure 1.1 illustrate the design and test GB. However, this GB restricts the performance and energy efficiency. To realize high performance with low power and high reliability, the optimization of the guard-band

for aging is important.

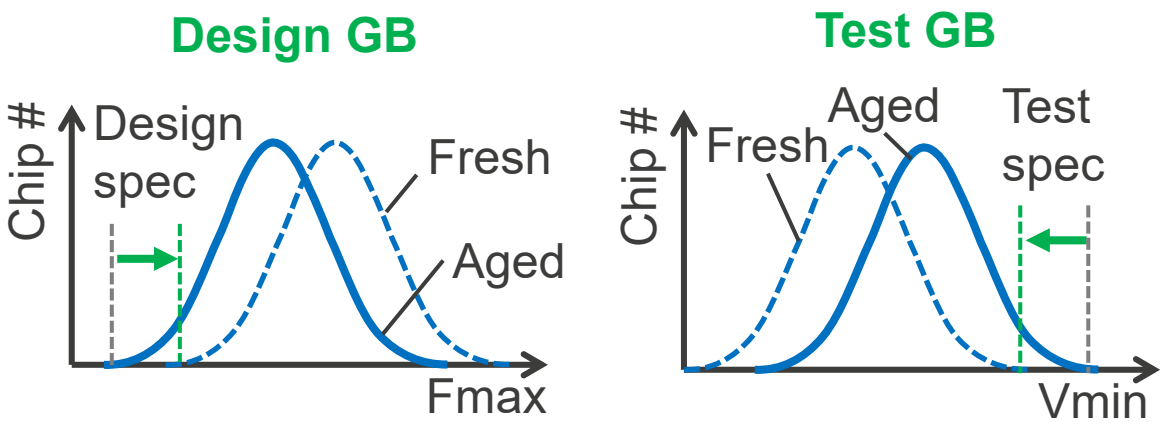


Figure 1.1 Design and test guard-band for aging

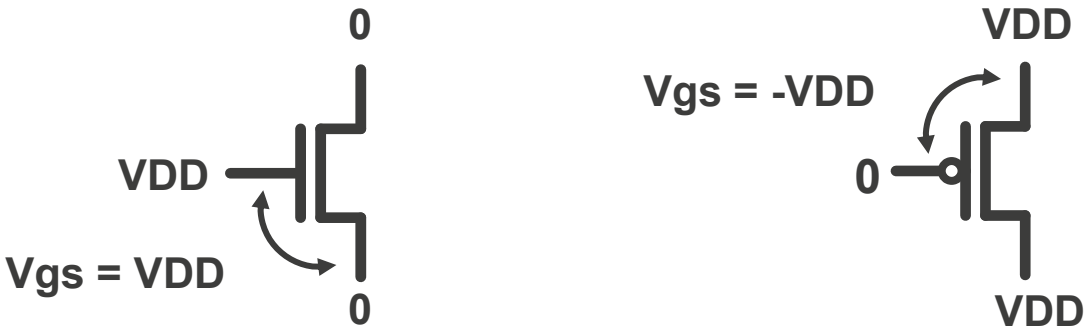
This study experimentally examines the variability of BTI by Ring Oscillator (RO) to realize optimal and robust Design-For-Reliability (DFR). The local layout effect of BTI caused by difference of layout pattern of each standard cell and on-chip local BTI variation are demonstrated and discussed. In addition, RO based on-chip aging monitors that consists only of a standard cells are proposed. Those measurement results include various process technology from 28 nm High-K Metal Gate (HKMG) to a 7 nm FinFET process. This study is intended to contribute to giving a more accurate guideline for DFR at advanced process technologies and intended to realize a reliable LSI system with on-chip aging monitors.

This chapter is organized as follows. Section 1.2 and 1.3 introduce the characteristics and the impact on circuits of BTI and HCI, respectively. Section 1.4 describe the challenges of Design for Reliability at Advanced LSI Design. Section 1.5 introduce the purpose of this study and section 1.6 shows the brief outline of this thesis.

1.2. Bias Temperature Instability

1.2.1. Characteristic of BTI

BTI is a phenomenon in which stress occurs during ON state at MOSFET, and its characteristics fluctuate with time. There are two types of BTI, one is Negative BTI (NBTI) and the other is Positive BTI (PBTI). As illustrated in Figure 1.2, NBTI stress is occurred in PMOS transistors with applying negative gate-source voltage (V_{gs}) [7][8] whereas PBTI is occurred in NMOS transistors with positive V_{gs} [9]. The PBTI degradation is increased since the High-K Metal-Gate (HKMG) process is applied after 40 nm technology nodes[10][11]. This is because the defects in the High-K layer of the gate oxide of NMOS increased as compared with those of the SiON.



(a) PBTI stress in NMOS (b) NBTI stress in PMOS

Figure 1.2 Schematic of bias condition of NBTI and PBTI stress

Figure 1.3 shows drain current vs. gate voltage (I-V) characteristics of fresh and aged device. The threshold voltage (V_{th}) and on current of a transistor are increased and decreased after BTI stress, respectively. This leads to decrease circuit performance such as increase of delay of logic circuit, increase of the minimum operation voltage (V_{min}) of a static random access memory (SRAM) and so on. According to Atomistic Trap-Based Model (ATB Model)[12], this fluctuation is caused by trapping and de-trapping of carriers into defects of gate oxide. If a carrier is captured in a defect, V_{th} is increased. The case of emission of carriers is vice versa. When a transistor turns on, the trapping becomes a dominant factor, resulting in performance degradation of the transistor.

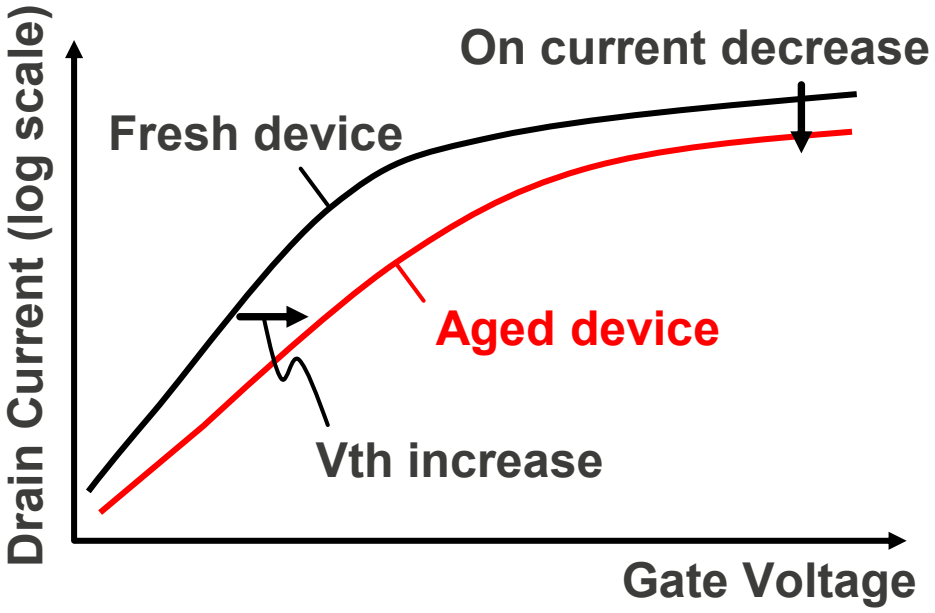


Figure 1.3 I-V characteristics of fresh and aged transistor

BTI causes not only performance degradation but also recovery. Figure 1.4 shows the time dependence of V_{th} degradation of NBTI according to V_{gs} as an example. The V_{th} degradation increases during a period when V_{gs} of PMOS is less than 0, whereas V_{th} is recovered if V_{gs} is greater than or equal to 0. This recovery effect occurs because the de-trapping becomes dominant under this bias condition. Note that since the BTI induced degradation has both permanent and recoverable elements, it is not fully recovered.

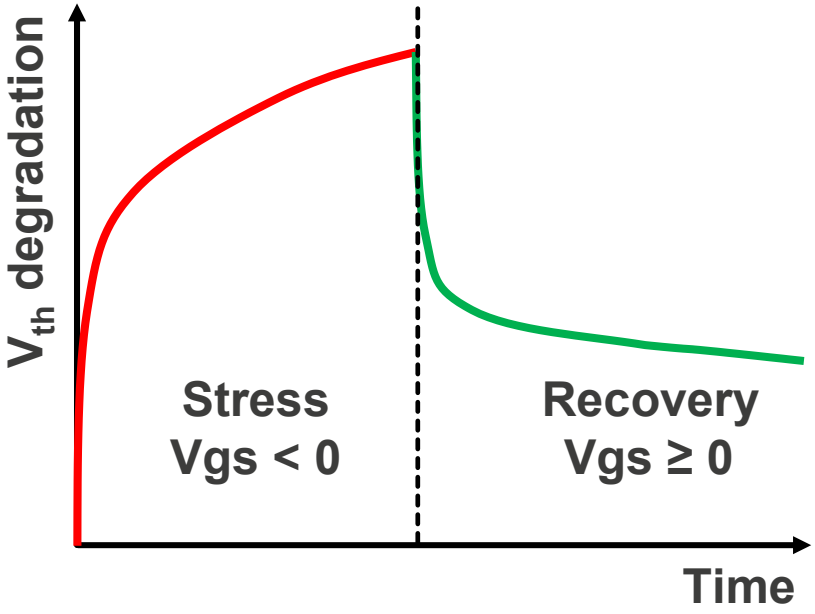


Figure 1.4 Stress and Recovery of NBTI

1.2.2. Impact of BTI on Logic Circuit

Figure 1.5 shows an example of relationship between circuit operation of an inverter and its BTI. When input voltage (Vin) of the inverter becomes high, output voltage (Vout) becomes low. In this scene, NMOS of the inverter is degraded by PBTI whereas NBTI degradation of PMOS is recovered. The case where Vin is low has the opposite characteristics of NBTI and PBTI. If Vin is continuously low during lifetime, meaning non-operation state, NBTI stress is only occurred and vice versa. If the switching operation of the circuit occurs continuously, meaning operation state, both NBTI and PBTI are occurred with the recovery effect. These stress conditions are called as "DC stress" and "AC Stress" in this thesis, respectively. In this way, Complementary Metal-Oxide Semiconductor (CMOS) circuit basically causes NBTI and/or PBTI degradation regardless of the operation and non-operation states although the stress condition of BTI such as recovery differs.

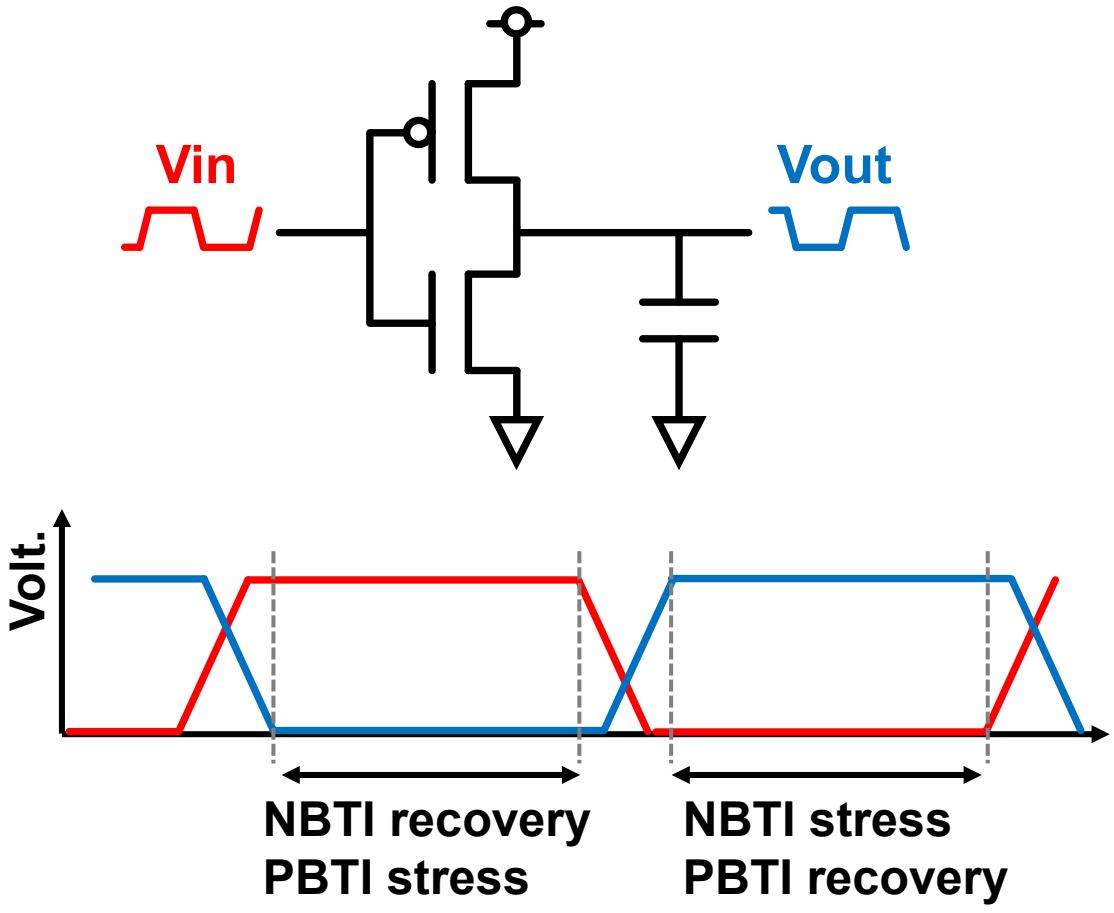


Figure 1.5 Relationship between circuit operation and BTI stress

1.3. Hot Carrier Injection

1.3.1. Characteristic of HCI

HCI is a phenomenon in which high energy (hot) carrier are injected into the gate oxide of MOSFET and cause characteristic degradation of the transistor [13]. The hot carrier is generated by acceleration due to the electric field between the drain and the source terminals. As illustrated in Figure 1.6, hot carriers are injected only when current flows between source and drain node. In

a scaled process node, higher V_{gs} lead to become larger HCI degradation. Figure 1.7 shows the worst bias condition of HCI in NMOS and PMOS at a scaled CMOS process.

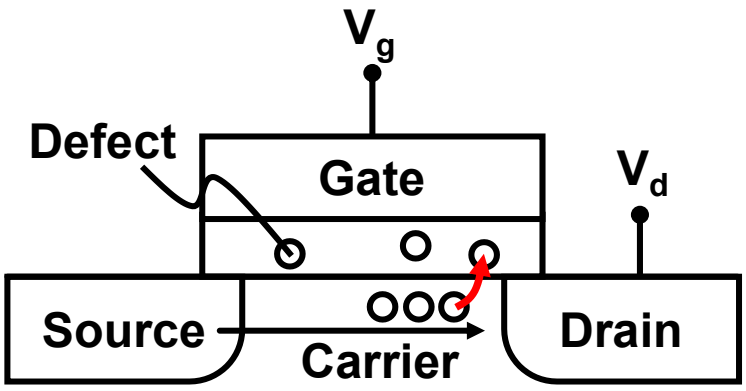
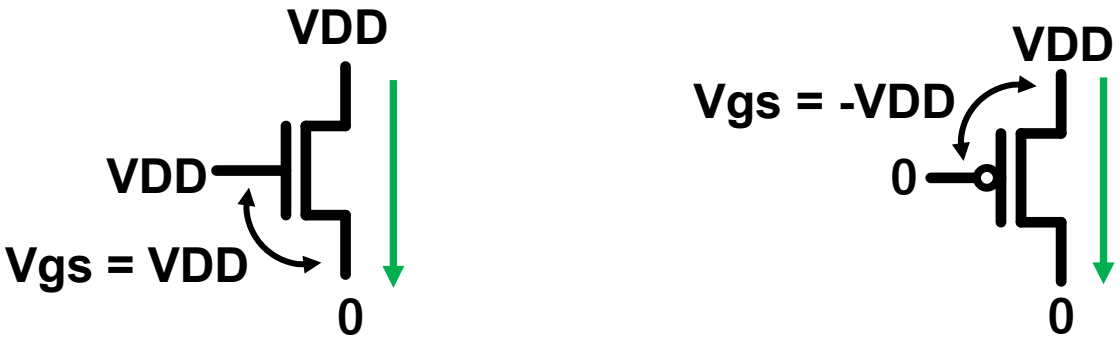


Figure 1.6 Schematic view of cross section of transistor and HCI



(a) HCI stress in NMOS

(b) HCI stress in PMOS

Figure 1.7 Schematic of the worst bias condition of HCI stress at scaled process

1.3.2. Impact of HCI on Logic Circuit

Figure 1.8 shows an example of relationship between circuit operation of an inverter and its HCI. Since HCI occurs only when current flows between source and drain, CMOS logic circuits have HCI during switching operation period. When *Vin* of the inverter changes from low to high, NMOS becomes ON and *Vout* becomes low. In this scene, NMOS of the inverter is degraded by NMOS HCI (nHCI). The case where *Vin* changes from low to high has PMOS HCI (pHCI). Since the deterioration due to HCI accumulates, the deterioration increases as the number of switching operations increases. The longer the transition time of output waveform is with same operation frequency, the bigger HCI is because of relative increase of stress time at the same operation time. Note that HCI has no recovery effect unlike BTI.

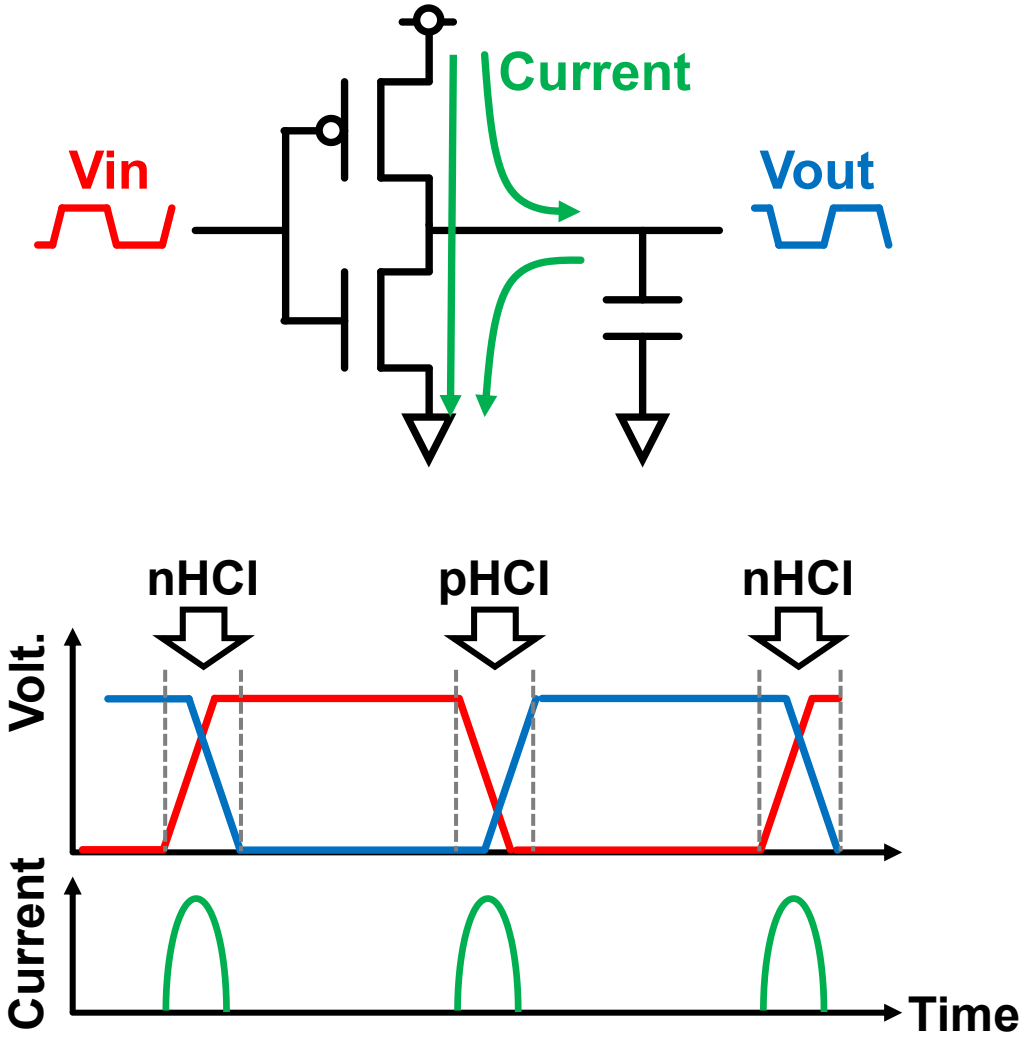


Figure 1.8 Relationship between circuit operation and HCI stress

1.4. Challenges of Design for Reliability at Advanced LSI Design

The device aging effects manifest themselves especially in scaled-down process technologies because of small design margin at low supply voltage (VDD) [14]. In the logic design point of view, there are many kinds of standard cells having different layout patterns such as Source/Drain length, distance between active areas, the number of fins, distance between gate contact and active edge in the logic circuits. The difference in characteristics of transistor caused by the difference in these layout patterns is so called Local Layout Effect (LLE) and it can affect not only time-0 characteristics of the transistor but also BTI-induced degradation. It is important to perceive the impact of LLE of BTI on logic circuits, especially for high reliability required applications. Several related studies have been published [15][16][17]. Investigating the influence of BTI's LLE in a wide range of standard cells will give a more accurate guideline for guard band design for logic circuits. In addition to LLE of BTI, there are time-0 variations due to process variations [18][19][20][21] and BTI induced variability especially in scaled process technology nodes [22][23][24][25]. The impact of these variabilities is increased with process technology scaling because of both increase of amount of variability and decrease of design margins. Therefore, considering both time-0 (before stress) process variation and local BTI variation (after stress) at cutting-edge process technologies is one of the key issues for robust design especially in automotive applications where high reliability is required for human safety.

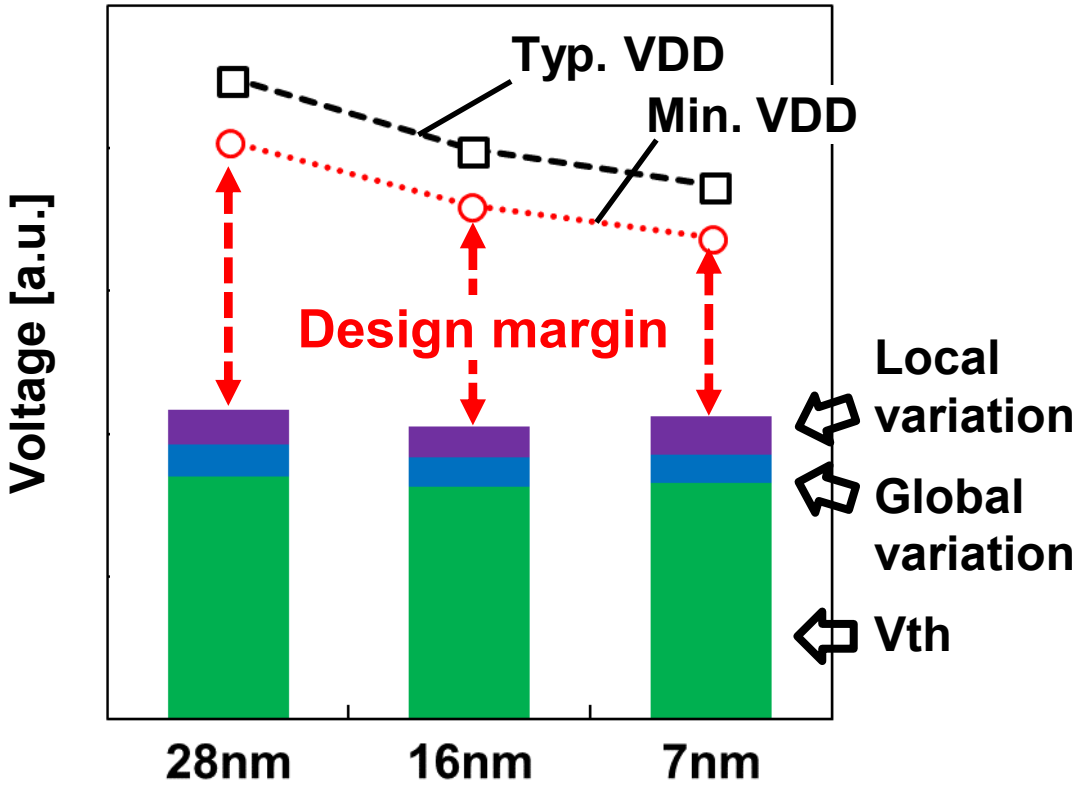


Figure 1.9 Supply voltage and design margin at advanced process

The dynamic voltage and frequency scaling (DVFS) technique [26][27][28][29] is often used in LSIs to optimize power efficiency at each operation scene and to get higher performance by voltage boost. However, voltage boost leads to increase aging degradation. In addition, the amount of aging degradation of each chip may vary because of chip mean variation of BTI and HCI. In other word, actual aging degradation of each chip may vary depending on each operation environment, DVFS usage, chip by chip variability of aging and so on. Therefore, an aging monitor system with on-chip aging monitor, which is easy to implement in products, could be a solution to optimize required GB and detect outlier of aging at testing [30].

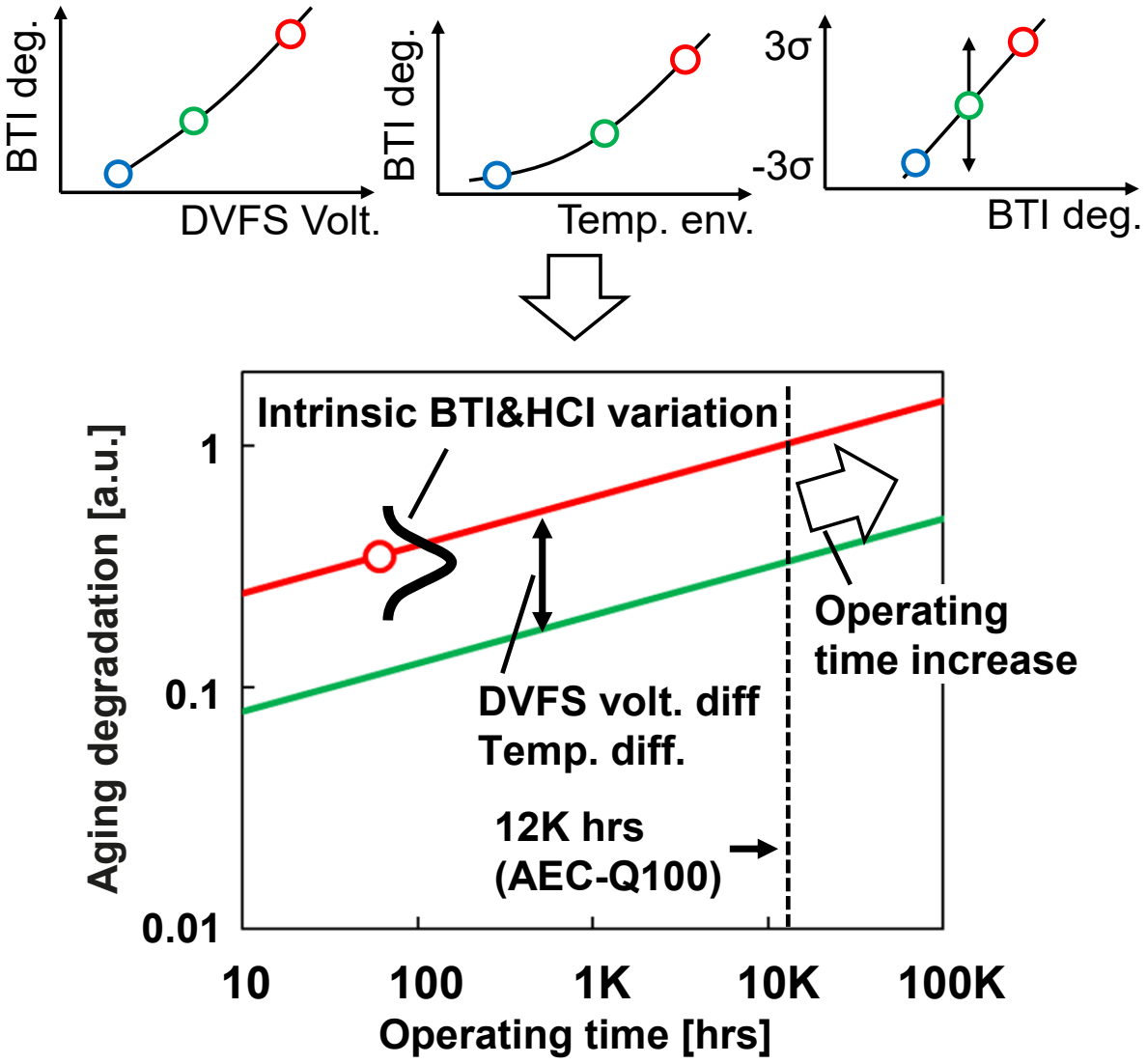


Figure 1.10 Fluctuations in aging due to voltage, temperature, operation time and variation

1.5. Purpose of this Study

In this study, the measurement results of characteristics of LLE on BTI and local BTI variation are demonstrated. Those impacts on circuit operation are also discussed. In addition, an highly sensitive on-chip digital aging monitor is proposed and measurement results are demonstrated.

1.6. Overview of this Thesis

Chapter 2 shows an analysis methodology of LLE of BTI on logic circuits by measuring various ROs consisted with many kinds of standard cells. The measurement results of impact of BTI's LLE including both degradation amount and recovery effect on a test chip fabricated in a 10nm FinFET process.

Chapter 3 shows an analysis of local variability of BTI by measuring Ring-Oscillators on various processes. The impact of local variability of BTI on logic circuit and SRAM are discussed.

Chapter 4 shows a fully standard cell based highly sensitive on-chip BTI and HCI monitor by unbalanced Ring-Oscillators. This monitor can separately monitor NBTI and PBTI.

Chapter 5 concludes this study.

Chapter 2 A Study of local layout effect on BTI

This chapter shows an analysis methodology of the impact of Local Layout Effect (LLE) of BTI on logic circuits by measuring Ring-Oscillators (RO) and measurement results of a test chip. Its impact on logic circuit design is also discussed.

2.1. Introduction

In autonomous driving era, it is inevitable to pursue higher performance for automotive LSIs such as advanced driver-assistance systems (ADAS), cognitive applications and so on [2][3]. The required higher performance should be achieved under limited power budget at high temperature condition of cars. It is because high power consumption requires a large and expensive cooling system. In addition, it consumes car's battery especially at electric vehicle (EV). High reliability is also required in automotive LSIs especially for autonomous driving era because car accidents directly affect human life and a paradigm shift of car usage by autonomous driving would be reliability more severe [3]. In this way, demand for both high energy efficiency and high reliability is one of key challenges for automotive application.

The high temperature condition of cars causes a big impact on both power consumption and reliability issue. The bias temperature instability (BTI) is one of the major reliability factors to degrade the performance, especially at high temperature condition. In general, LSI designers take BTI guard-band into account to prevent delay failures at the end of the products lifetime although this guard-band leads to restrict the performance and energy efficiency. To achieve high performance with low power, optimization of the BTI guard-band is required to meet with high reliability requirement of automotive LSIs.

In logic design point of view, there are many kinds of standard cells having different layout patterns such as S/D length, distance between active areas, the number of fins, distance between gate contact and active edge in the logic circuits. A characteristic of a transistor at time-0 (before stress) strongly depends on the difference of layout patterns in a scaled process. In addition to time-0 characteristic, it is important to perceive the impact of LLE of BTI on logic circuits, especially for such applications that require high reliability, and several studies have been published [15][16][17]. Investigating the influence of BTI's LLE in a wide range of standard cells will give a more accurate guideline for guard band design for logic circuits. In this chapter, the analysis

methodology of LLE of BTI on logics circuit is presented. This analysis methodology is based on measured data of various ROs consisted with many kinds of standard cells.

This chapter is organized as follows. In Section 2.2, configuration of the test chip for analysis of LLE of BTI is introduced. Section 2.3 discusses the analysis methodology of LLE of BTI on various ROs. Section 2.4 shows measurement and analysis results of a test chip fabricated in a 10 nm FinFET process. Based on the measurement result, the impact of LLE of BTI on logic circuit design is discussed. A brief summary of this Chapter is presented in Section 2.5.

2.2. Test Chip Configuration in 10 nm FinFET Process

Figure 2.1 and Figure 2.2 show a die photo and block diagrams of the test chip fabricated in a 10 nm FinFET bulk CMOS technology [15]. In “Block A”, there are 64 kinds of ROs composed of various standard cells, drive strength and Fan-Out number (F.O.) with 61 stages to measure BTI degradation with different layout patterns. The cell type covers Inverter (INV), Buffer (BUF), 2~4 input NAND, 2~4 input NOR, multiplexer (MUX), complex gate of and-or-invert with two of two-input (AOI22) and Delay cell. As for drive strengths in INV and BUF, 0.7x, 1x, 4x, 8x and 16x are implemented and dependency of active Fin length can be evaluated, where “x” stands for drivability. In “Block B”, there are 128 ROs composed of the same configuration with 9 stages to measure the variation caused by BTI under the same layout effect.

Each RO has a 2 input NAND or NOR cell for oscillation control gate. One of ROs is selected and activated through the decoder and measure oscillation frequency with the counter one by one. All ROs share a common counter, and each RO have dedicated frequency divider described as “divider” in Figure 2.2. Because it is necessary to lower the oscillation frequency of each RO to transmit it to the common counter. Note that all ROs in both block A and B are measured one by one in order to sufficiently suppress a power supply noise caused by oscillation. Although the stage number of RO in Block B is not a prime number, the harmonic noise has not been observed at all in this measurement environment.

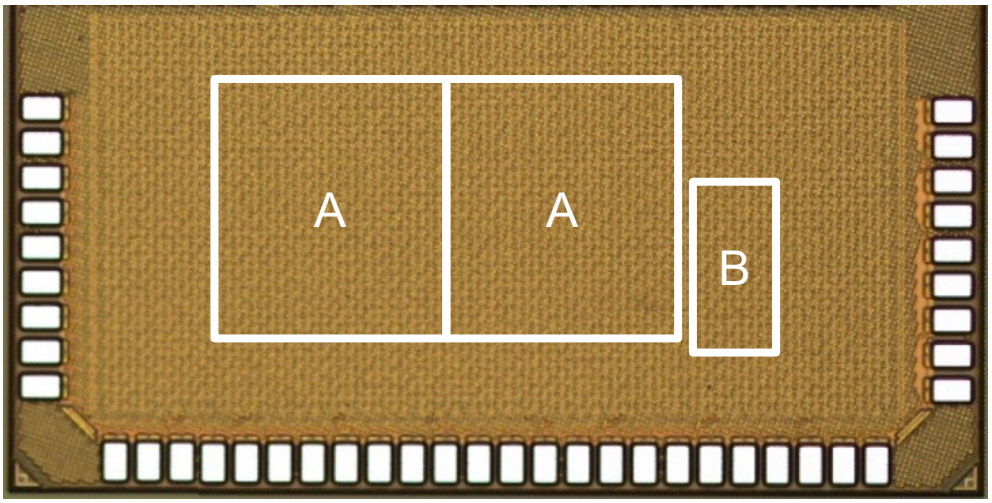


Figure 2.1 Die photo of test chip in a 10 nm FinFET bulk CMOS process

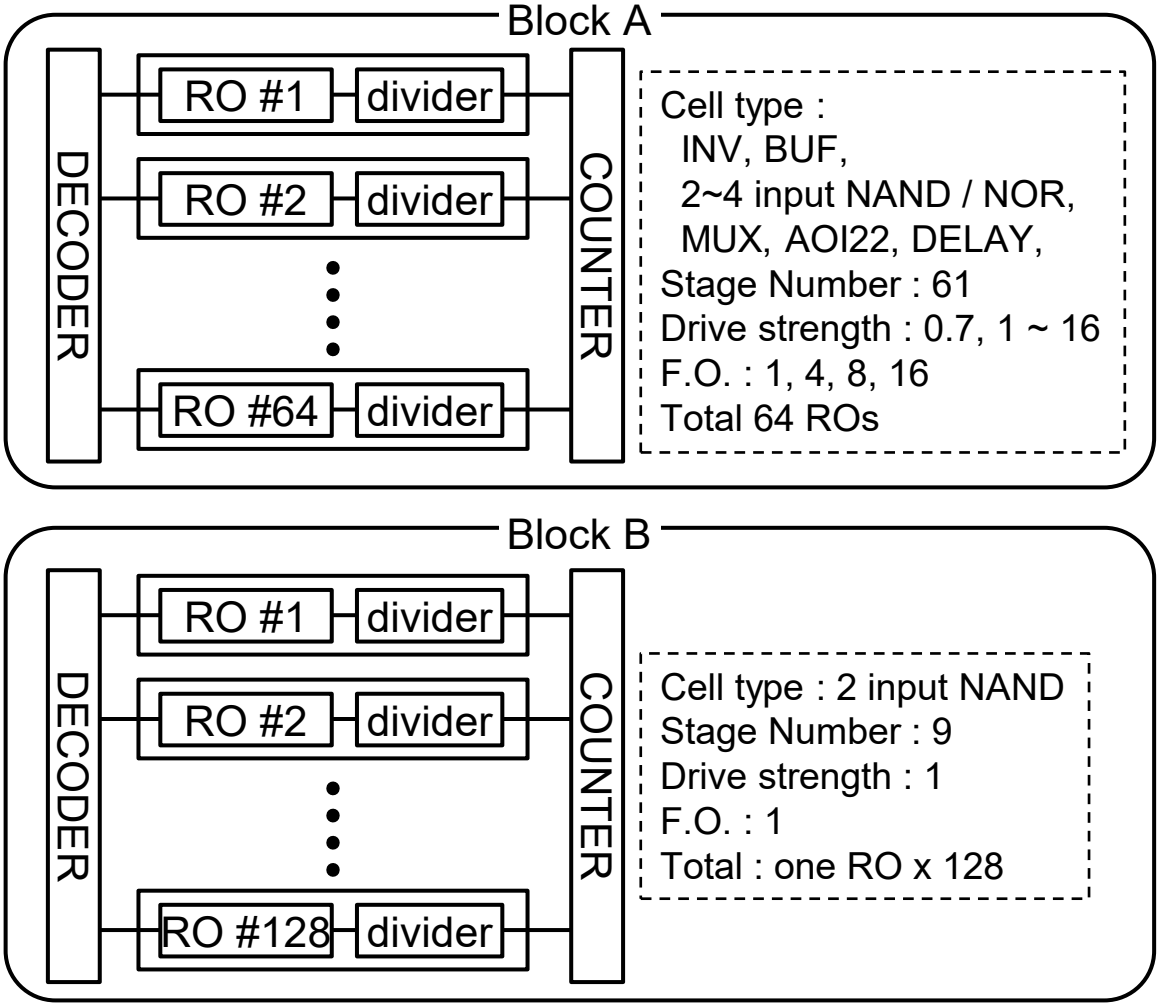


Figure 2.2 Block Diagram of test chip in a 10 nm FinFET bulk CMOS process

Figure 2.3 shows a timing diagram of supply voltage (VDD) which is applied to the test chip. *Tpd* means the inverse of the oscillation frequency of RO. Four conditions of *Tpd* are measured as shown in red square: (a) fresh measurement as a reference, (b) stress phase measurement only at Block B, (c) initial measurement after stress for suppressing BTI recovery effect, (d) measure recovery effect by power-down period to accelerate recovery. Both Block A and B are measured except stress phase. A high voltage and high temperature stress are applied to all ROs during stress phase at non-oscillation condition (DC stress). A definition of total recovery the time "Trec" is the sum of the period in which VDD is 0V. *ΔTpd* is the ratio of aged *Tpd* to fresh one. *ΔTpd(0)* and *ΔTpd(Trec)* are defined as the deviations measured at condition (c) and condition (d), respectively. The monitor voltage for measuring Tpd is set to be lower than stress voltage because the impact of BTI on *ΔTpd* is relatively increased with decreasing VDD due to decrease of gate overdrive voltage "$V_{gs} - V_{th}$".

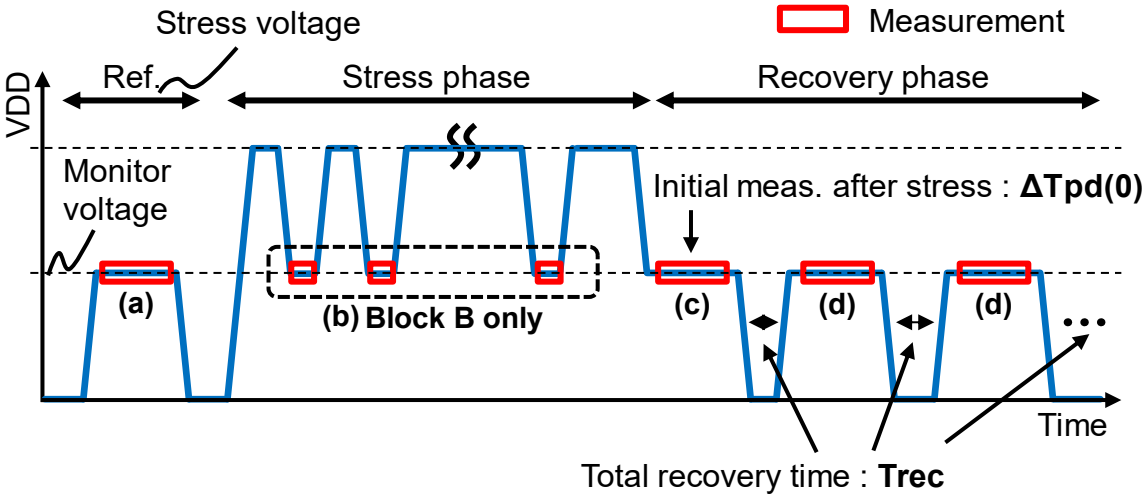


Figure 2.3 Measurement waveform of supply voltage

2.3. Analysis Methodology of Local Layout Effect on BTI

The basic concept of an analysis methodology of LLE on logic circuits utilizes the difference of impacts of BTI on its delay in each standard cell type. It is known that the BTI impact on logic circuit performance depends on its circuit configuration [31] even if there is no BTI's LLE on each standard cell type. Figure 2.4 shows BTI sensitivity on each RO's delay and ratio of delay affected by BTI. The bar graph is the ratio of the amount of delay affected by BTI to the total delay, and the line graph is the BTI sensitivity. The horizontal axis indicates configuration of each RO; the first one is standard cell type, the second is drive strength "X", the third is F.O. (e.g. f08 means F.O. is 8) and the last is a drive pin if the cell has multiple input-pins such as 2-input NAND. As shown in Figure 2.4, each RO has different Positive BTI (PBTI) sensitivity α and Negative BTI (NBTI) sensitivity β. α is $\partial \Delta Tpd/\partial V_{thn}$ and β is $\partial \Delta Tpd/\partial V_{thp}$, where V_{thn} and V_{thp} are V_{th} of NMOS and PMOS, respectively. Figure 2.5 shows examples of schematic views of ROs and its bias condition at the DC stress condition. BTI sensitivity differs depending on the standard cell type, which is caused (i) by the difference of delay ratio affected by BTI, and (ii) by the stacked NMOS and PMOS effect.

In case of BUF RO with 8 times drivability (buf X8), the 1st stage INV (1st-INV) in BUF has a smaller drivability than output stage INV (out-INV). If F.O. is 1, delay of 1st-INV becomes larger than that of out-INV because of larger load capacitance of 1st-INV. As F.O. increases, delay of out-INV increases, results in decrease of ratio of 1st-INV delay to the total delay. As for BTI stress, since the input signal of 1st-INV becomes high during DC stress, PBTI degradation is occurred in 1st-INV. As a result, BUF with large drive strength has relatively large PBTI sensitivity compared with other RO configuration and this PBTI sensitivity decreases with increasing F.O. as shown in Figure 2.4. Note that the sum of the delay of the two graphs in Figure 2.4 is less than 100%. This is because, only one rise or fall edge of input signal in each cell is affected by PBTI or NBTI whereas the opposite edge is not during the DC stress condition. As for (ii), in the case where the drive pin of 2-input NAND is allocated close to the output node (pin A), and if the voltage of pin A is changed from 0V to VDD, source-drain voltage of NMOS with tie-high pin B increases with increasing voltage of pin A. This induces lower gate-source voltage V_{gs} of driving NMOS than non-stacked case such as Inverter during the transient period, resulting in higher V_{thn} sensitivity on its delay because of smaller gate-overdrive-voltage "V_{gs} - V_{thn}". This stacked NMOS and PMOS effects are increased with increasing the number of stacked MOS.

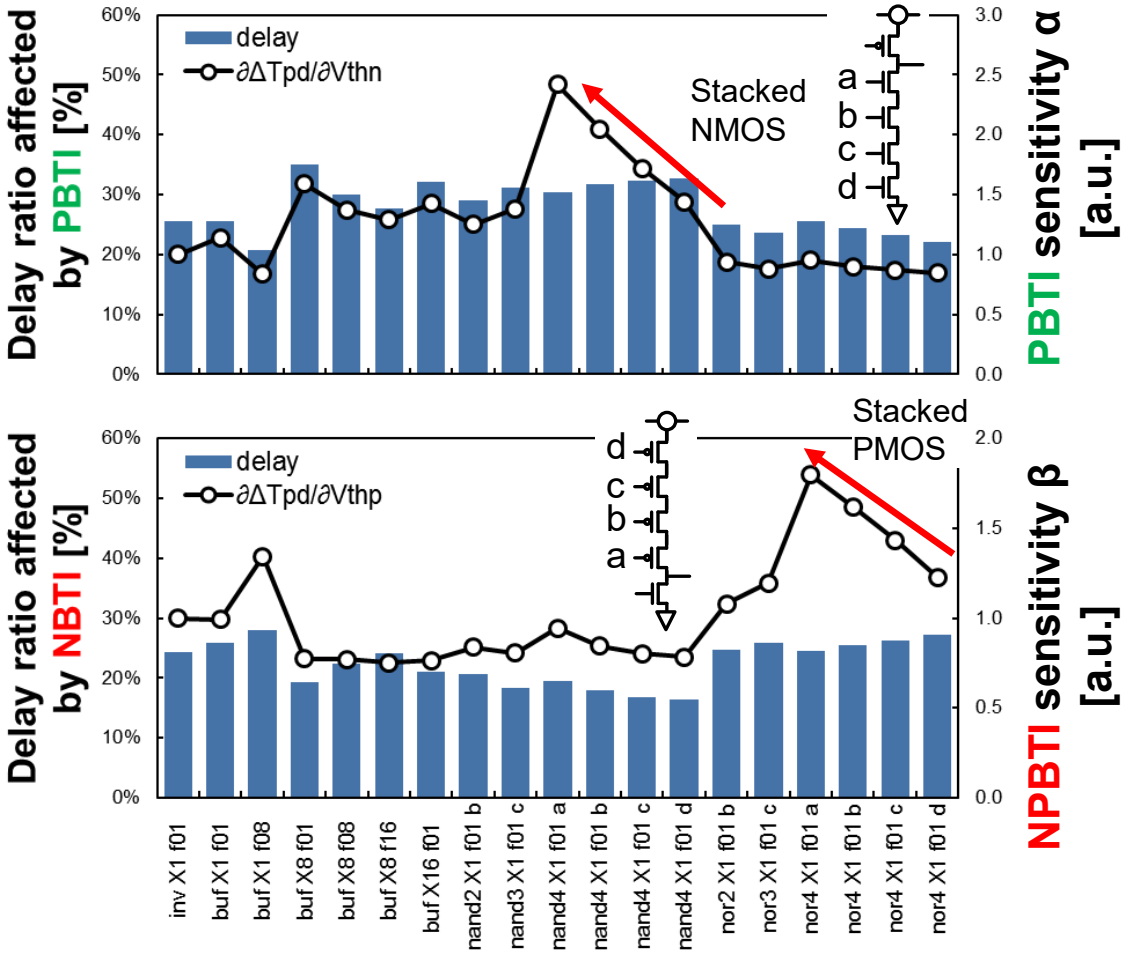


Figure 2.4 BTI sensitivity difference of various standard cells

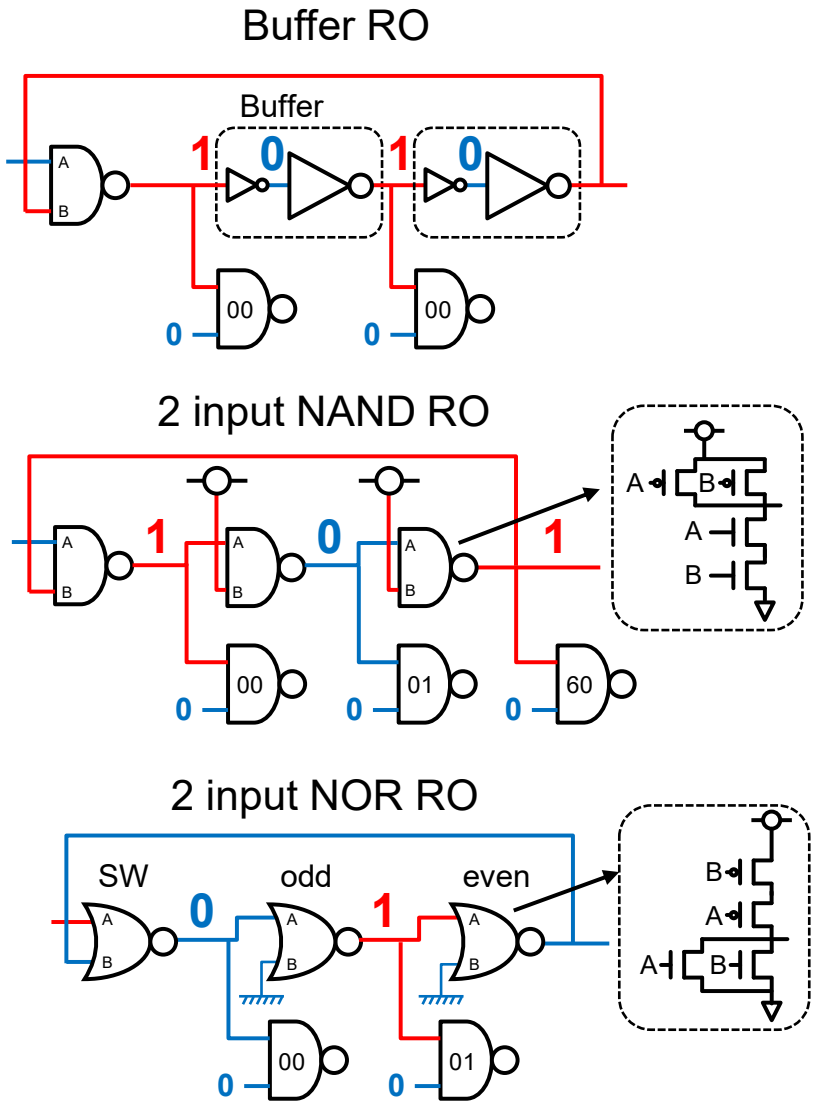


Figure 2.5 Examples of schematic of ROs and its bias condition under DC stress

Figure 2.6 shows the estimation methodology of V_{thn} and V_{thp} degradation (ΔV_{thn} and ΔV_{thp}) by using BTI sensitivity difference of each RO. The "#1", "#2", "#3", "#4" and "#5" as shown in figure 2.6 mean chip identification number. Two type of input data are required for this analysis one is (1) measured Tpd degradation of each RO ($\Delta Tpd(0)_k$) and other is (2) estimated BTI sensitivity α and β by simulation as shown in figure 2.4. The Tpd degradation of each RO is estimated by the following equation:

$$\Delta Tpdest_k(\Delta V_{thn}, \Delta V_{thp}) = \alpha_k \Delta V_{thn} + \beta_k \Delta V_{thp} \qquad (2\text{–}1)$$

where, α_k and β_k stand for simulated PBTI and NBTI sensitivity of each RO, respectively. The linearity and additivity of Eq. (2-1) of each RO are confirmed by simulation as shown in figure 2.7. ΔV_{thn} and ΔV_{thp} are estimated from Eq. (2-1) and measured Tpd degradation of each RO (ΔTpd_k) by Least-Square-Method (LSM).

$$\varepsilon = \sum_{k=0}^{63} \left(\Delta Tpd(0)_k - \Delta Tpdest_k(Vthn, Vthp)\right)^2 \qquad (2\text{–}2)$$

where, ε is residual sum of squares (RSS) and the minimum point of ϵ is solution of ΔV_{thn} and ΔV_{thp}. Then $\Delta Tpdest_k$ of each RO can be obtained from the ΔV_{thn} and ΔV_{thp} derived by LSM and Eq. (2-1). These $\Delta Tpdest_k$ do not correctly include BTI's LLE of each standard cell. It is because $\Delta Tpdest_k$ of each RO is estimated by the same ΔV_{thn} and ΔV_{thp} at each chip. If the influence of BTI's LLE is large, actual ΔV_{thn} and ΔV_{thp} of each RO should have variability. As a result, the estimated $\Delta Tpdest_k$ and the measured $\Delta Tpd(0)_k$ should have a large discrepancy.

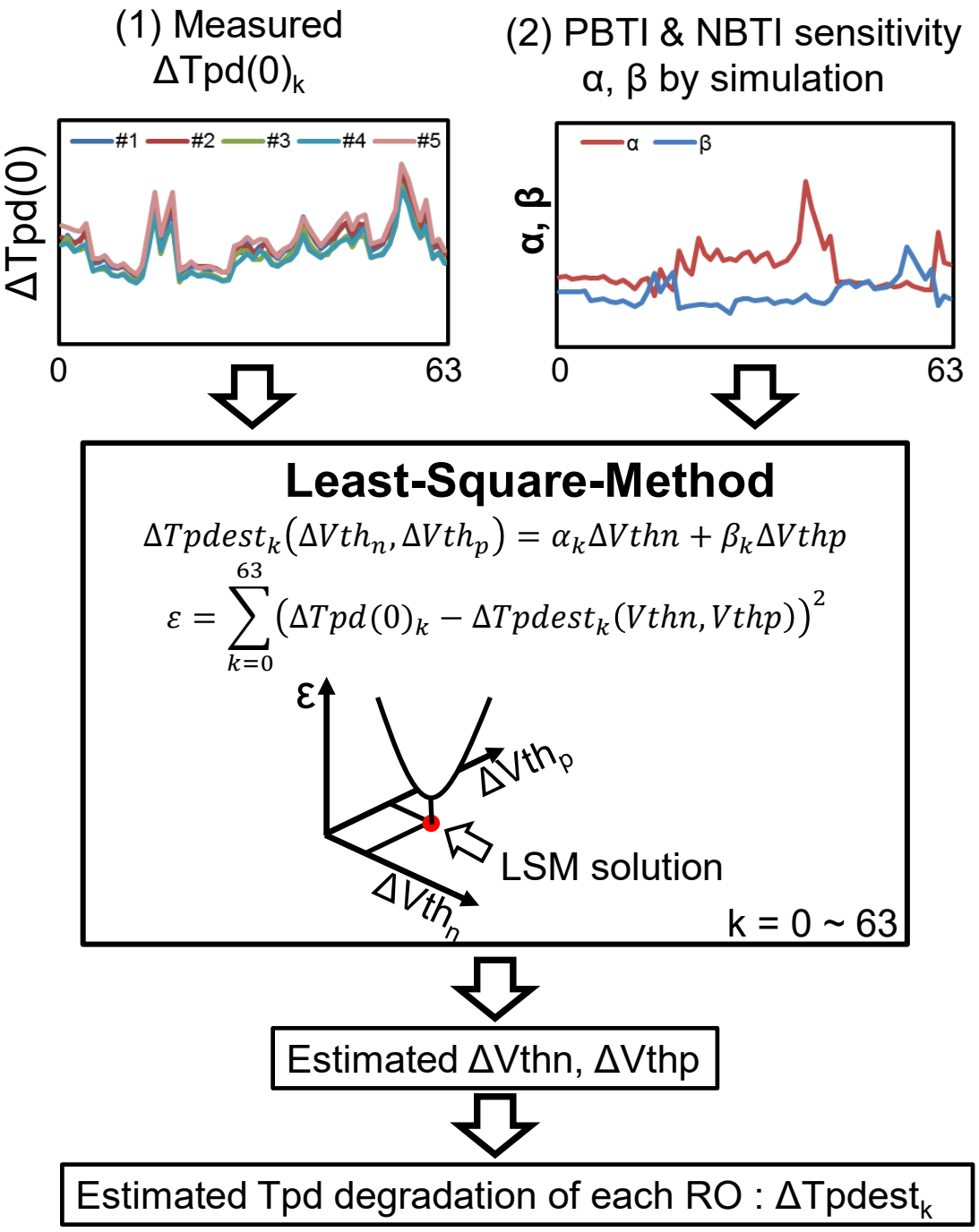


Figure 2.6 ΔV_{th} and *ΔTpdest* estimation methodology from measured *ΔTpd* and simulated BTI sensitivity

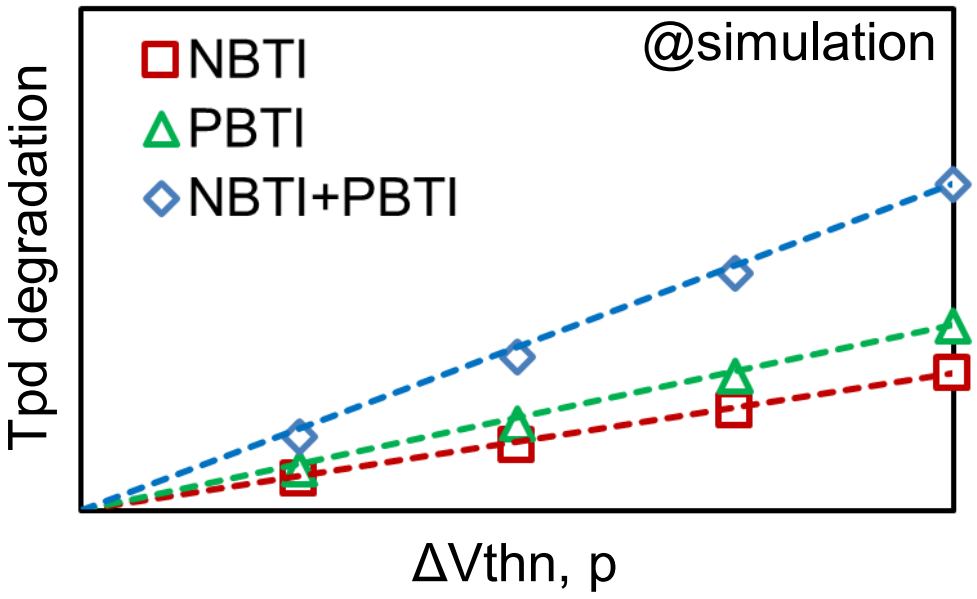


Figure 2.7 An examples of Linearity and Additivity of Eq. (2-1)

2.4. Measurement and Analysis Results

Figure 2.8 shows the estimated ΔV_{th} based on analysis methodology described in Figure 2.6. This result shows PBTI is significantly smaller than NBTI, agreeing with the similar result of reference [15] of relatively low voltage stress. Figure 2.9 shows comparison between measured and estimated Tpd degradation of all ROs by using estimated ΔV_{th}. 5 chips are measured and each chip has two "Block A", thus 10 blocks of each RO are measured in total. The range of measured $\Delta Tpd(0)$ is from 6% to 17%, which is caused by the difference of BTI sensitivity in each RO. The dotted line means that measured ΔTpd is equal to estimated one. The points above the dotted line show that estimated ΔTpd is underestimated, and underlying plots show overestimation. The measured and estimated values are well correlated and a correlation coefficient between them is 0.955. The error rate which is the deviation of the measured value from the estimated value is -19% and +18% in minimum and maximum, respectively.

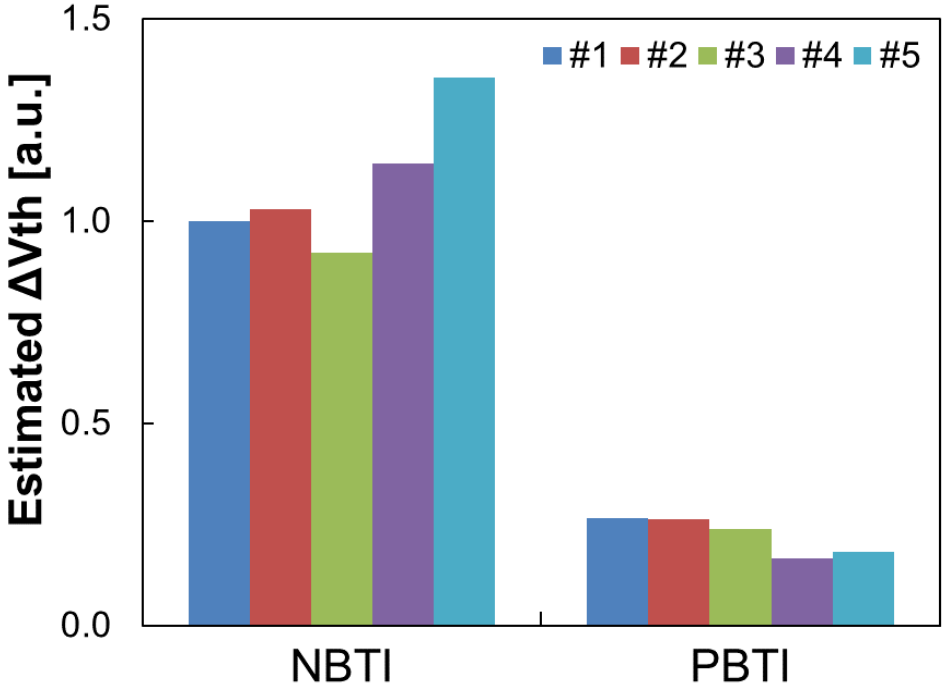


Figure 2.8 Estimated ΔV_{th} of BTI

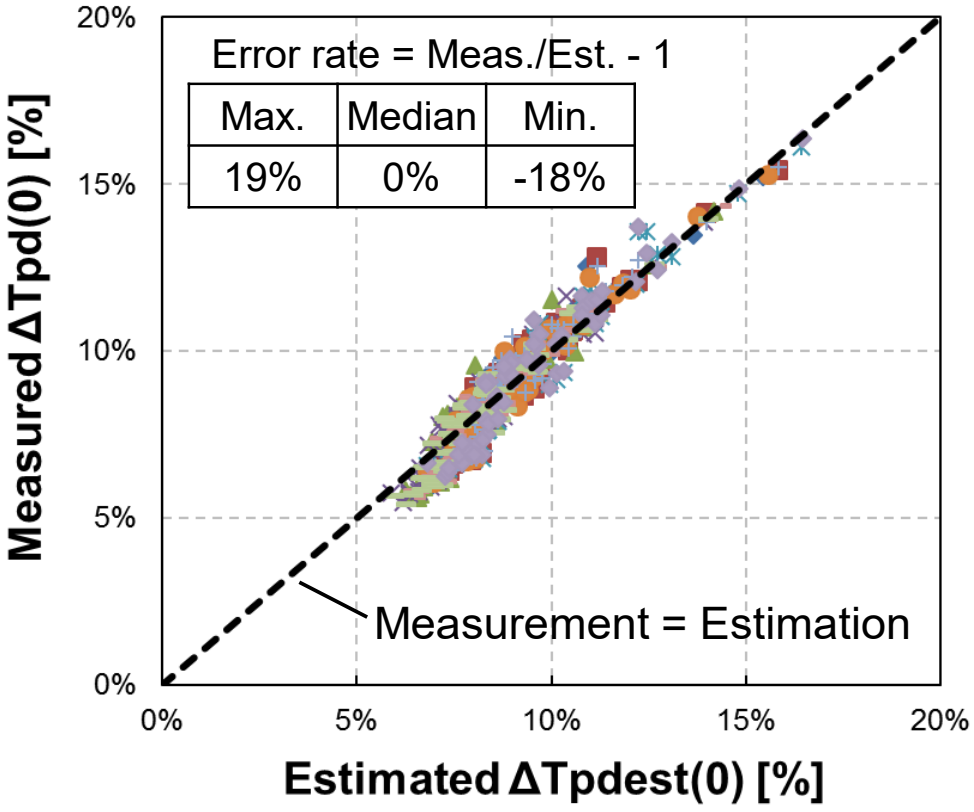


Figure 2.9 Comparison of measured and estimated ΔTpd

Since BTI has statistical variability even if the layout pattern is same, the error rate shown in Figure 2.9 includes this intrinsic BTI variation. Figure 2.10 shows measurement results of BTI variation of 128 ROs with 9-stages to confirm its impact. It can be confirmed that the variation distributions of the 5 chip measurement results show same tendency. The estimated *ΔTpd* variation normalized by the median value is 22% at 3σ based on measurement results. It is known that the intrinsic BTI variance is proportional to the reciprocal square root of the number of Fins [15], and it can be replaced to the number of stages of RO if the drive strength of each cell is the same. Therefore, the variation amount of the 61-stage RO at 3σ becomes 8.5%. From this result, the intrinsic statistical BTI variation in Figure 2.9 cannot be ignored.

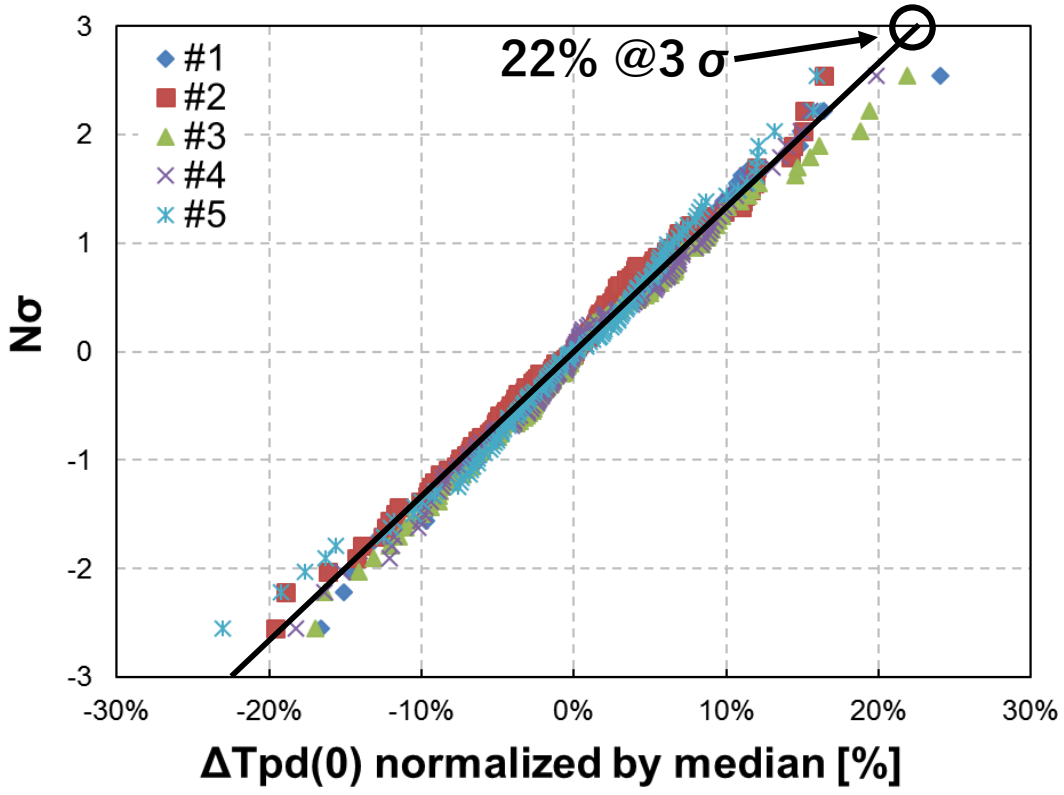


Figure 2.10 Measured BTI variation of 9-stage ROs

To remove the intrinsic BTI variation component as much as possible from the BTI's LLE analysis result shown in figure 2.9, the median value of 10 measurement points of each RO is used. Figure 2.11 shows the breakdown of the median error rate of 10 measured values of each cell type

configuration. The overall maximum and minimum error rates caused by BTI's LLE are -16% at Buffer with large drive strength and +13% at Inverter with small drive strength cell, respectively. Larger error rate means larger BTI degradation and smaller error rate is vice versa. Focusing on the result of each drive strength of INV and BUF, BTI decreased with increasing drive strength. In other word, long active length [15] leads to decrease BTI degradation. This result shows that if the BTI guard-band is estimated based on estimated ΔV_{thn} and ΔV_{thp} shown in Figure 2.8, there is possibility that a -16% to +13% discrepancy may be occurred by BTI's LLE depending on the cell configuration.

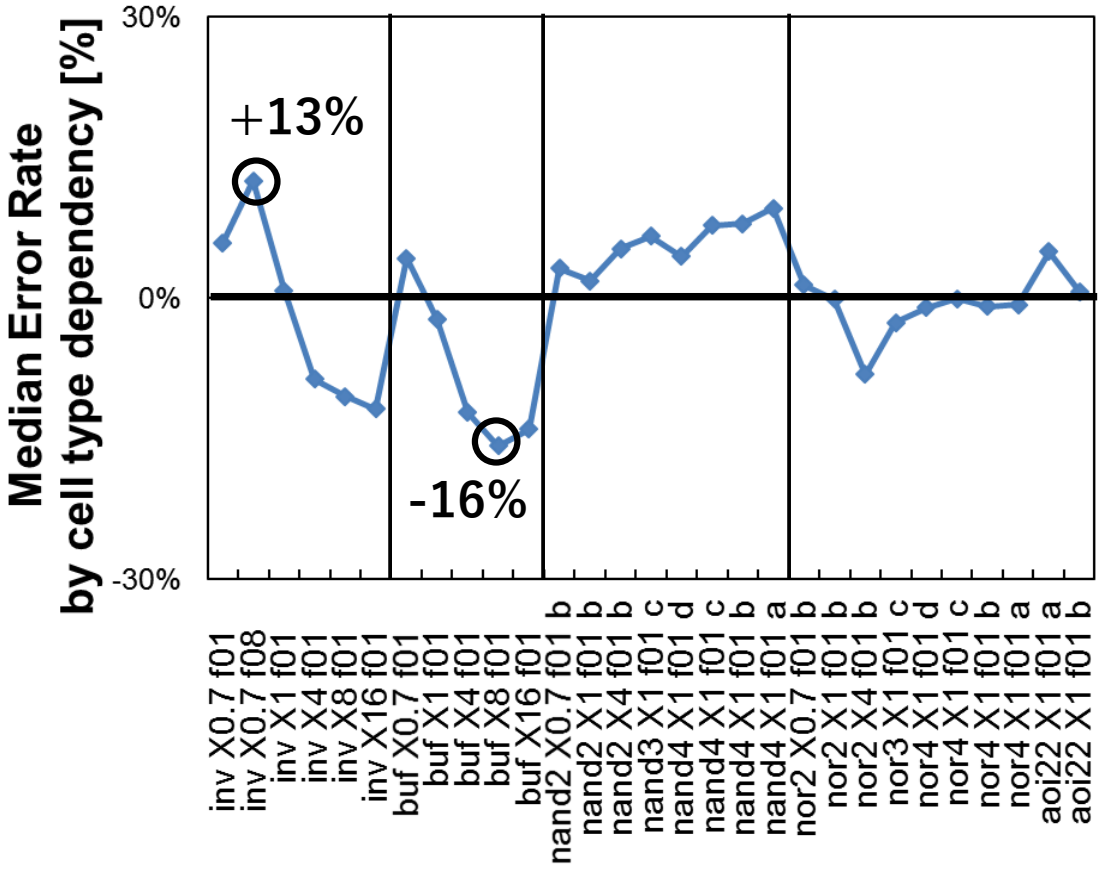


Figure 2.11 Breakdown of cell type dependency on median error rate between measured and estimated BTI degradation

INV and BUF cells with large drive strength have large active length [15] and are generally used in clock line. Therefore, the impact of these BTI's LLE on the logic circuit depends on its clock structure. If there is almost no clock skew on the logic circuit, the delay degradation of clock line does not affect the setup timing. On the other hand, in case of having large clock skew, the

increase of clock skew would make setup timing be degraded depending on whether increase of clock skew lead to decrease setup timing margin or not. Other combinational cells frequently used in data line such as NAND, NOR and AOI22 do not show significant impact of BTI's LLE in the setup timing point of view. This is because those cells do not have significant impact of LLE on BTI and are generally used randomly in data line. The cell type dependency of BTI would be able to be considered by a commonly-used technique such as On Chip Variation (OCV) methodology [32][33] which is used in typical timing design of Static Timing Analysis (STA) by a commercial EDA tool for considering process variation. In case of applying delay margin due to BTI by OCV and if the OCV for BTI is set depending on drive strength of each cell, BTI's LLE obtained at this test chip can be taken into acount in logic design.

The impact of LLE on the recovery effect of BTI is also evaluated because it is important to reflect this effect to the guard-band based on the actual circuit operation. The recovery factor is defined by the deviation of ΔTpd(100sec) from ΔTpd(0) where ΔTpd(100sec) is Tpd degradation after turning off VDD for 100 seconds in total. As shown in Figure 2.12, there is no obvious dependency on the standard cell type difference. The median recovery factor of all standard cell type is 0.76 and the maximum difference from median value in the same chip is less than ± 0.03. This result indicates that there is enough accuracy for BTI guard-band design of complexed logic circuit to take into account the median recovery effect of the many standard cell type in this 10nm FinFET process. In this way, the impact of LLE on BTI including the recovery effect can be experimentally evaluate and its impact on logic circuit design can be handled by the OCV design methodology.

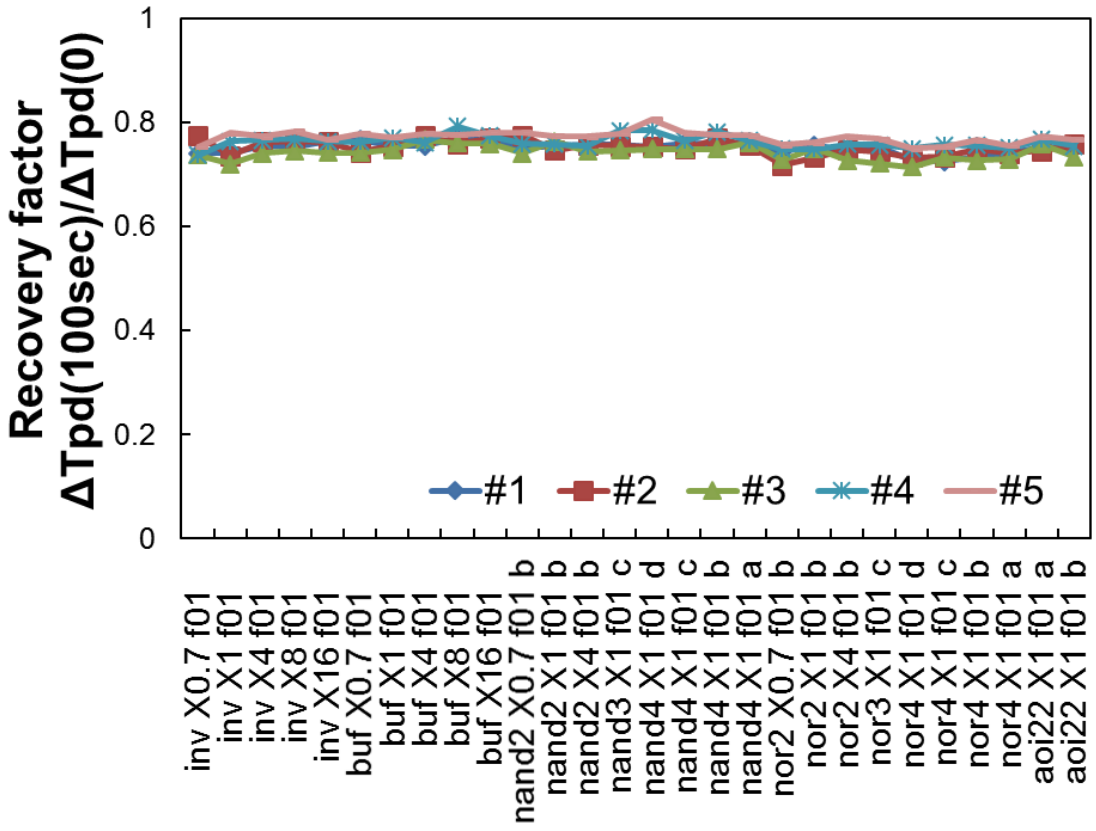


Figure 2.12 Breakdown of median error rate of cell type dependency

2.5. Summary

The analysis methodology of LLE of BTI by measuring various ROs having different BTI sensitivity is introduced in this chapter. The measurement results of the test chip fabricated in a 10 nm FinFET are shown and analysis results are discussed. The performance degradation of each standard cell is well matched to the estimated one without considering LLE and the maximum error rate of median measurement values is from -16% to +13%. The LLE impact on the recovery effect of BTI is also discussed and there is no significant dependency on standard cell type. These analyses would be helpful to design BTI guard-band with considering BTI's LLE in logic circuits for high reliability required applications.

Chapter 3 A Study of local BTI variation with Ring-Oscillator in Advanced Process

This chapter shows an analysis of local variability of bias temperature instability (BTI) by measuring Ring-Oscillators (RO) on various processes. The evaluation results based on measuring ROs of a test elementary group (TEG) fabricated in 7 nm FinFET process, 16/14 nm generation FinFET processes and a 28 nm planar process show that the standard deviations of NBTI V_{th} degradation ($\sigma(\Delta V_{thp})$) are proportional to the square root of the mean value ($\mu(\Delta V_{thp})$) at any stress time, V_{th} flavors and various recovery conditions. While the amount of local BTI variation depends on the gate length, width and number of fins, the amount of local BTI variation at the 7 nm FinFET process is slightly larger than other processes. Based on these measurement results, the impact of local BTI variation on logic circuit and SRAM are discussed.

3.1. Introduction

As described in chapter 2.1, optimization of the guard-band for aging is required to realize high performance with low power and high reliability especially in scaled-down process. The device aging effects such as BTI manifest themselves especially in scaled-down process technologies because of small design margin at low supply voltage (VDD) [14]. In addition to time-0 variation due to process variation [18][19][20][21], there is BTI induced variability especially in scaled process technology node [22][23][24][25]. Therefore, considering both time-0 (before stress) process variation and local BTI variation (after stress) at cutting-edge process technologies is one of the key issues for robust design in automotive applications where high reliability is required for human safety.

This chapter organized as followings. Section 3.2 introduces the structure of a test elementary group (TEG) and its measurement methodology. Section 3.3 describes the measurement results and discussions. In Section 3.4, the analysis results of impact of local BTI variation on logic circuit and static random access memory (SRAM) in 7 nm FinFET are described. A brief conclusion is given in Section 3.5.

3.2. Test Chip for Local BTI Variation

In section 3.2, a test chip structure fabricated in a 7nm FinFET bulk CMOS technology and its measurement condition are described.

Figures 3.1 and 3.2 show a block diagram and a die photo of a TEG including lots of ring oscillators (ROs) to measure BTI degradations. The circuit diagram of Figure 3.1 shows a state of 0 or 1 of each node when ROs stop oscillation. The red and blue schematics illustrate that each cell has Negative BTI (NBTI) or Positive BTI (PBTI) stress during non-oscillation condition, respectively. The purpose of "Block A" and "Block B" is to measure on-chip variation and chip mean BTI degradation, respectively. The main difference between "Block B" in Figure 2.2 and "Block A" in Figure 3.1 is that the latter also has cells of different V_{th} types and cell heights. In "Block A", there are 128 9-stage-ROs with 2-input NAND cells with 3 flavors of V_{th} and 2 types of cell heights to measure both time-0 variation and local BTI variation. As for the cell-height type, one includes two fins per finger and the other four fins per finger. One of the input signals of each NAND cell is fixed to VDD except for the control cell. As illustrated in the red and blue schematics in Figure 3.1, this circuit configuration is affected by both NBTI and PBTI during non-oscillation condition. In "Block B", there are two types of ROs; NOR-RO and NAND-RO. They can fix all outputs to high or low respectively by EN or ENB that can apply NBTI or PBTI stress only on each RO [34][35]. These ROs have 61 stages to measure chip mean NBTI or PBTI degradation with local BTI variation suppressed. It is because if on-chip BTI variation is a random phenomenon like time-0 variation, it can be averaged over a large stage number of ROs. Note that there is four different chips with similar configurations fabricated in two different 16/14 nm generation FinFET processes called 16/14 nm Gen. process-A and process-B respectively and in a 28 nm planar process. In this chapter, unless otherwise noted, the measurement results of TEG in a 7nm FinFET bulk CMOS technology are shown.

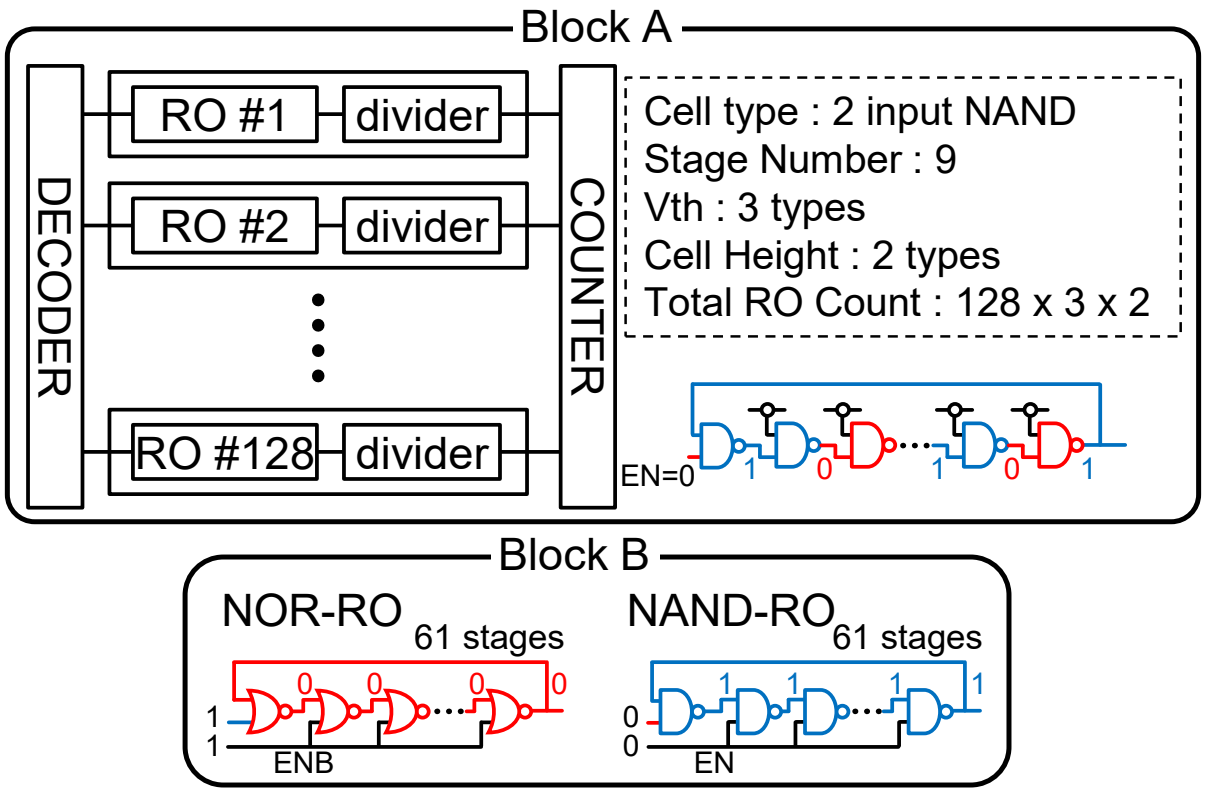


Figure 3.1 Block diagram of TEG in 7 nm FinFET process

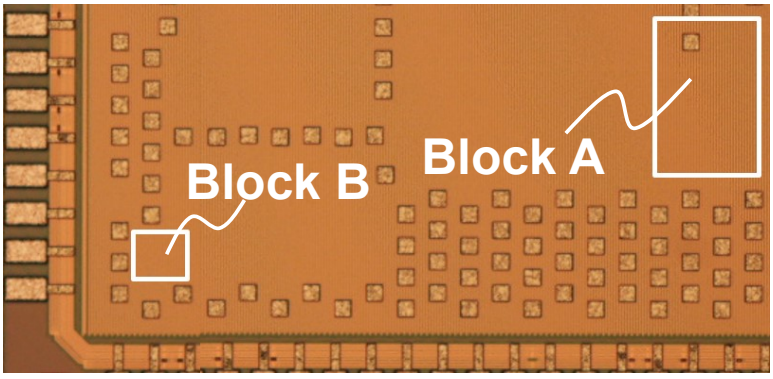


Figure 3.2 Die photo of TEG in 7 nm FinFET process

Figure 3.3 shows a schematic waveform of VDD which is applied to the TEG. Tpd means the inverse of the oscillation frequency (F) of RO. Tpd is measured at 4 conditions as shown in red squares: (a) fresh measurement as a reference (Tpd0 or F0), (b) stress phase measurement, (c) initial measurement after stress for suppressing BTI recovery effect, (d) measurement with recovery by power-down to accelerate recovery. A high voltage and high temperature stress with several hours stress are applied to all ROs during stress phase at non-oscillation condition (DC stress). This total amount of stress is intended to cover the expected field stress of the product. Stress voltage is more than 1.5 times higher than the monitor voltage, where oscillation frequency is measured at the monitor voltage. Tpd is measure only for "Block A" in the stress phase. ΔTpd and ΔF are the difference between fresh and aged Tpd and operation frequency F, respectively. The monitor voltage for measuring oscillation frequency is set to be lower than the stress voltage because the impact of BTI on $\Delta Tpd/Tpd0$ and $\Delta F/F0$ is relatively increased with decreasing VDD due to decrease of the gate overdrive voltage "$V_{gs} - V_{th}$". Note that all ROs are sequentially measured one by one to sufficiently suppress a power supply noise caused by the oscillation and ROs besides oscillated one are suspended. As a result, no harmonic noise was observed although the stage number of RO in "Block A" is not a prime number. The measurement time of each RO is around 200 μs and the interval between each RO is around 10 μs.

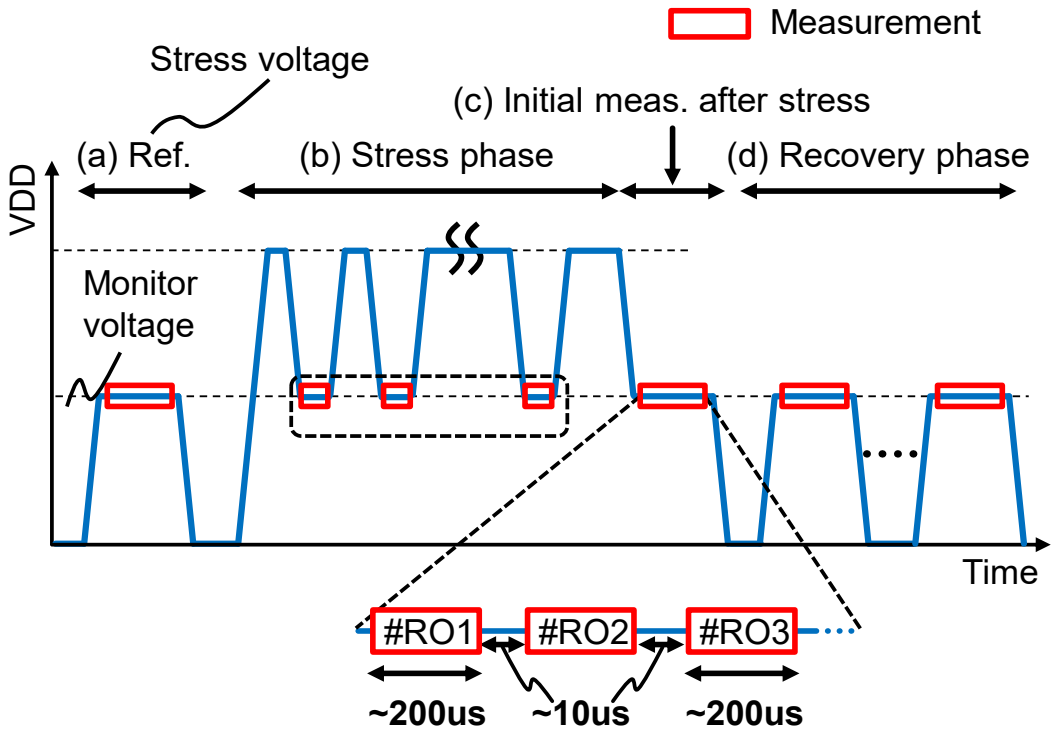


Figure 3.3 Measurement waveform of supply voltage, measurement time and interval

3.3. Measurement Results and Analysis Methodology

In this section, the measurement result and its analysis results of both chip mean BTI degradation and BTI induced local variation are described.

3.3.1. Chip Mean Degradation of BTI

The chip mean V_{th} degradation (ΔV_{th}) of NBTI and PBTI are estimated based on measurement results of ROs by using the following equation:

$$\Delta Tpd/Tpd0 = \alpha \Delta Vthn + \beta \Delta Vthp \quad (3\text{-}1)$$

where ΔV_{thn} and ΔV_{thp} mean estimation results of PBTI and NBTI induced V_{th} degradation, ΔTpd and Tpd0 mean measured Tpd degradation and fresh one, and α and β mean simulated PBTI and NBTI sensitivity factors of each RO, respectively. For example, α is calculated from the simulated ΔTpd when the V_{th} of the stressed NMOS is increased by a certain amount of ΔV_{thn}. The parameter α and β are varied depending on circuit configuration of each RO [35] and V_{th} flavor. The linearity and additivity of Eq. (3-1) of each RO are confirmed by SPICE simulations [35]. Since NBTI or PBTI stress can be selectively applied on NOR-RO and NAND-RO under DC stress as described in section 2, α of NOR-RO and β of NAND-RO are equal to 0. As a result, ΔV_{thn} and ΔV_{thp} are separately estimated by measuring NOR-RO and NAND-RO. Figure 3.4 shows chip mean BTI degradation of 6 chips normalized by MVT NBTI. MVT, LVT and ULVT mean flavors of V_{th} and represent medium, low and ultra-low V_{th} transistors, respectively. #1 to #6 indicate measurement chip identification numbers. As a result, in 7 nm, lower V_{th} transistors cause larger NBTI and ULVT is exposed to the worst NBTI. These results are similar result in ref. [36][37] in case of V_{th} modulation using metal gate work function (MWF). Figure 3.5 illustrates the band diagrams as V_{th} decreases by NWF and doping [38]. The physical mechanism is that as V_{th} decreases due to MWF tuning, the conduction band offset to the gate oxide decreases and the electric field across the gate dielectric increases. As a result, NBTI degradation increases [38]. In case of V_{th} modulation by doping, V_{th} dependency on NBTI is vice versa.

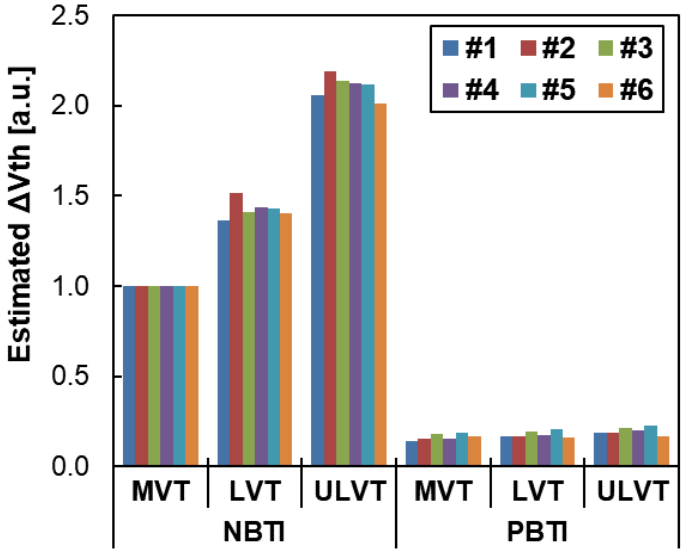


Figure 3.4 Block diagram of TEG in 7 nm FinFET process

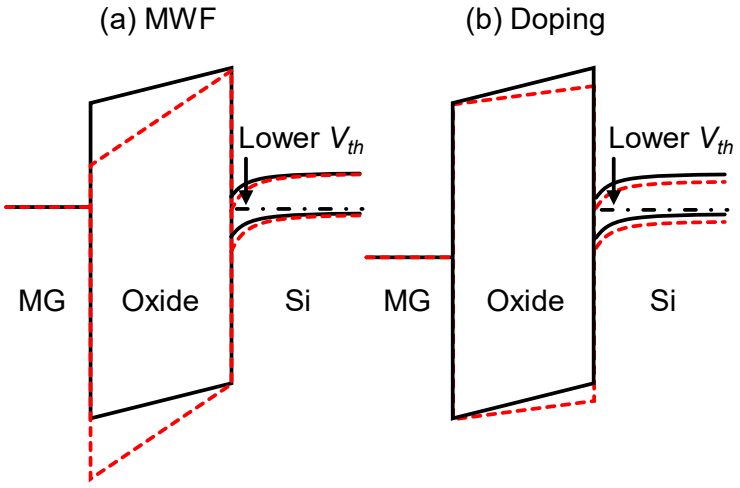


Figure 3.5 Gate field difference due to different V_{th} modulation methodology in NMOS; (a) metal gate work function vs. (b) doping

Figure 3.6 shows dependency of chip mean ΔV_{thp} on gate overdrive voltage "$V_{gs} - V_{thp}$" (Vov) normalized by MVT to analyze V_{th} dependency on NBTI. The dotted line is a line of exponential approximation. Note that V_{th} value of the horizontal axis is measured from Device Under Test (DUT) of PMOS transistors in this TEG. As a result, the ΔV_{thp} of each V_{th} flavor can be well explained with exponential approximation of Vov as described in ref. [38]. ULVT has around 2.1x larger chip mean NBTI than MVT. In case of PBTI, it is significantly smaller than NBTI in all V_{th} flavors, indicating the similar result in ref. [39][40][41][42]. This is caused by decrease of the electrical field across the gate dielectric in FinFET at the same Vov due to less depletion charge in the strong inversion of its fully depleted structure.

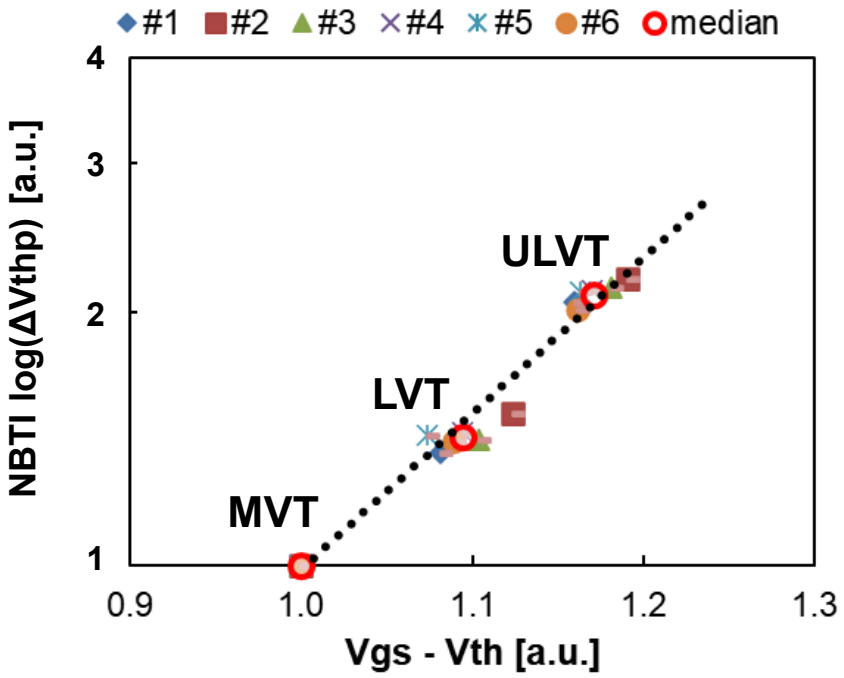


Figure 3.6 V_{th} dependency on NBTI ΔV_{thp}

Figure 3.7 shows chip mean BTI degradation of each TEG normalized by each NBTI of MVT. When comparing NBTI and PBTI in each process, PBTI is significantly smaller than NBTI at 16/14 nm Gen. process-A, 16/14 nm Gen. process-B and 28 nm planar as same as 7 nm FinFET. Note that as for the 28 nm process MVT and LVT transistors are only implemented in the TEG. Therefore, NBTI and PBTI of ULVT of 28 nm process are not available (N/A) in Figure 3.7.

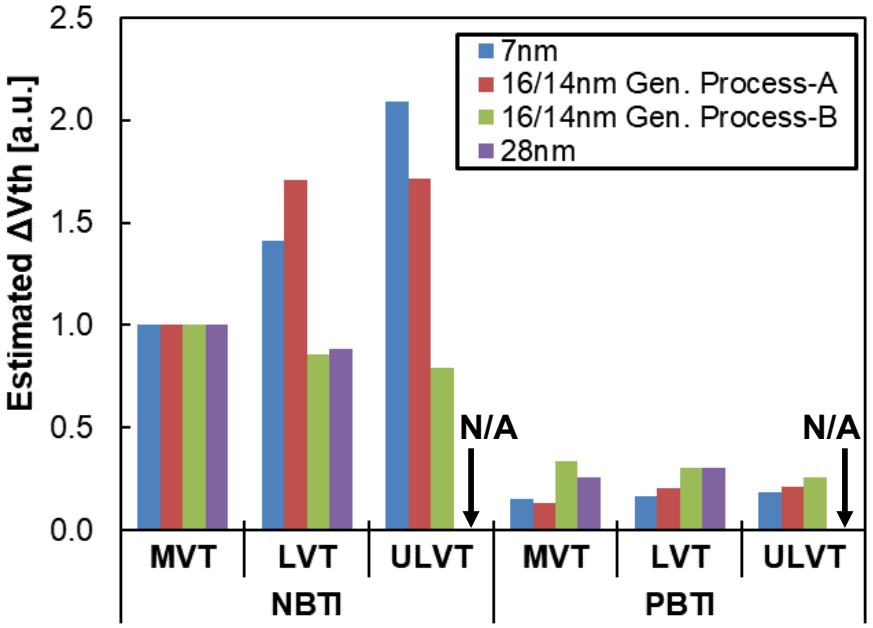


Figure 3.7 V_{th} dependency on NBTI ΔV_{thp}

3.3.2. Local BTI Variation

Figure 3.8 shows dependency of ΔF of 128 ROs of "Block A" on its measurement order and its correlation coefficient. The numbers on the horizontal axis in Figure 3.8 (a) indicate the measurement order of the 128 ROs. Since each RO is measured one by one with around 200 μs measurement time and 10 μs interval, each RO has different wait time before measurement. Therefore, there is a concern that the BTI recovery effect may vary, depending on the measurement order. However, since the correlation coefficient between each ΔF and the measurement order is smaller than 0.2 as shown in Figure 3.8 (b), all measurement results of ΔF for each RO do not change by measurement order. From this result, the recovery effect of each measurement result can be treated as almost the same.

Figure 3.9 demonstrates stress time and recovery time dependency on ΔF/F0 of 128 ROs of "Block A" in the 7 nm TEG. ΔF is measured with different stress time from 30 seconds to 8 hours in case of 7 nm TEG. After 8 hours stress, stress is released for 100 seconds in total by power off. The red bold line is drawn on the median values of 128 ROs and the other lines are measured results of each RO. The measured ΔF/F0 follows a power-low model to stress time "t" as in Equation (3-2)

$$\frac{\Delta F}{F0} = t^n \tag{3-2}$$

where "n" is time dependency factor "n". Its measured result is around 0.173 calculated by the median values. Figure 3.10 shows results of other processes whereas the minimum stress time of 16/14 nm Gen. process-B and 28 nm TEGs is extended to 0.5 seconds to evaluate a characteristic of local BTI variation when BTI degradation is relatively small. The ratio of the maximum and minimum values to the median value of ΔF/F0 decreases as the stress time increases in all measurement results.

Figure 3.11 shows distribution of ΔF at each stress time. It is not appropriate for evaluation of BTI variation to directly compare ΔF variation of different V_{th} flavors. It is because even if the degradation of BTI of each V_{th} flavor is the same, the ΔF of different V_{th} flavors is not the same due to the difference of Vov of each V_{th} flavor. For example, ΔF decreases with increasing Vov at constant ΔV_{th}. To address it, ΔF is converted to ΔV_{th}. Since NBTI is dominant compared to PBTI as shown in Figure 3.7, it is assumed that ΔTpd is proportional to NBTI degradation. The measured ΔTpd is converted to ΔV_{thp} as in Equation (3-3).

$$\frac{\Delta Vthp}{\mu(\Delta Vthp)} = \frac{\Delta Tpd/Tpd0}{\mu(\Delta Tpd/Tpd0)} \tag{3-3}$$

where $\mu(\Delta Tpd/\Delta Tpd0)$ is measured mean $\Delta Tpd/Tpd0$, and $\mu(\Delta V_{thp})$ is estimated mean ΔV_{thp} from Eq. (3-1) and measured ΔTpd of NOR-RO.

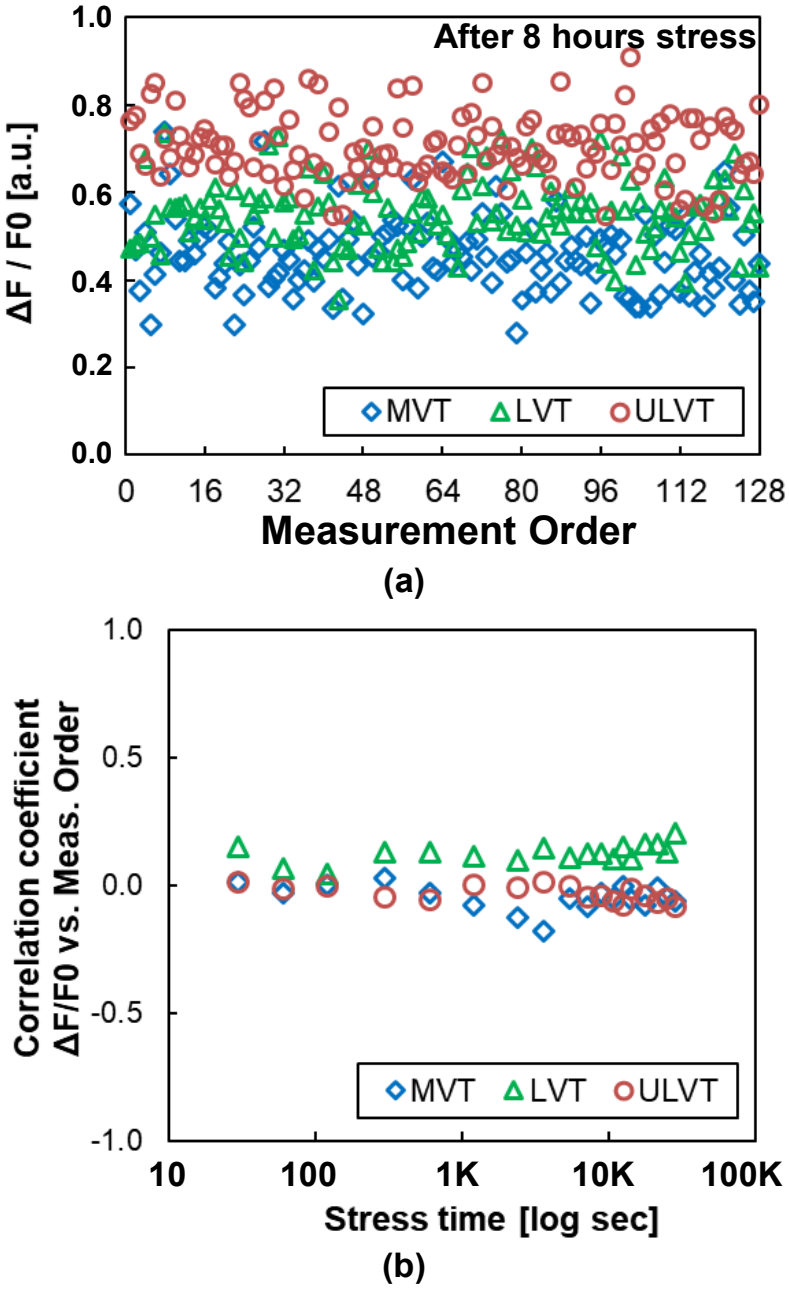


Figure 3.8 Correlation between degradation of oscillation frequency of ROs and measurement order in “Block A”

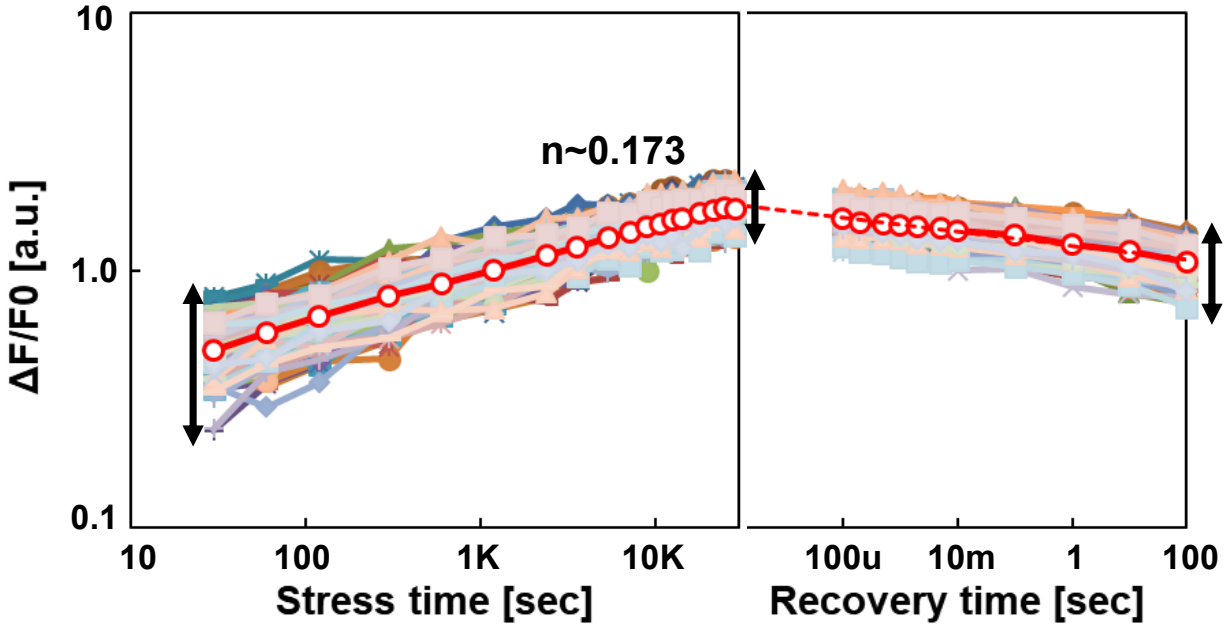


Figure 3.9 Stress time and recovery time dependency on oscillation frequency degradation

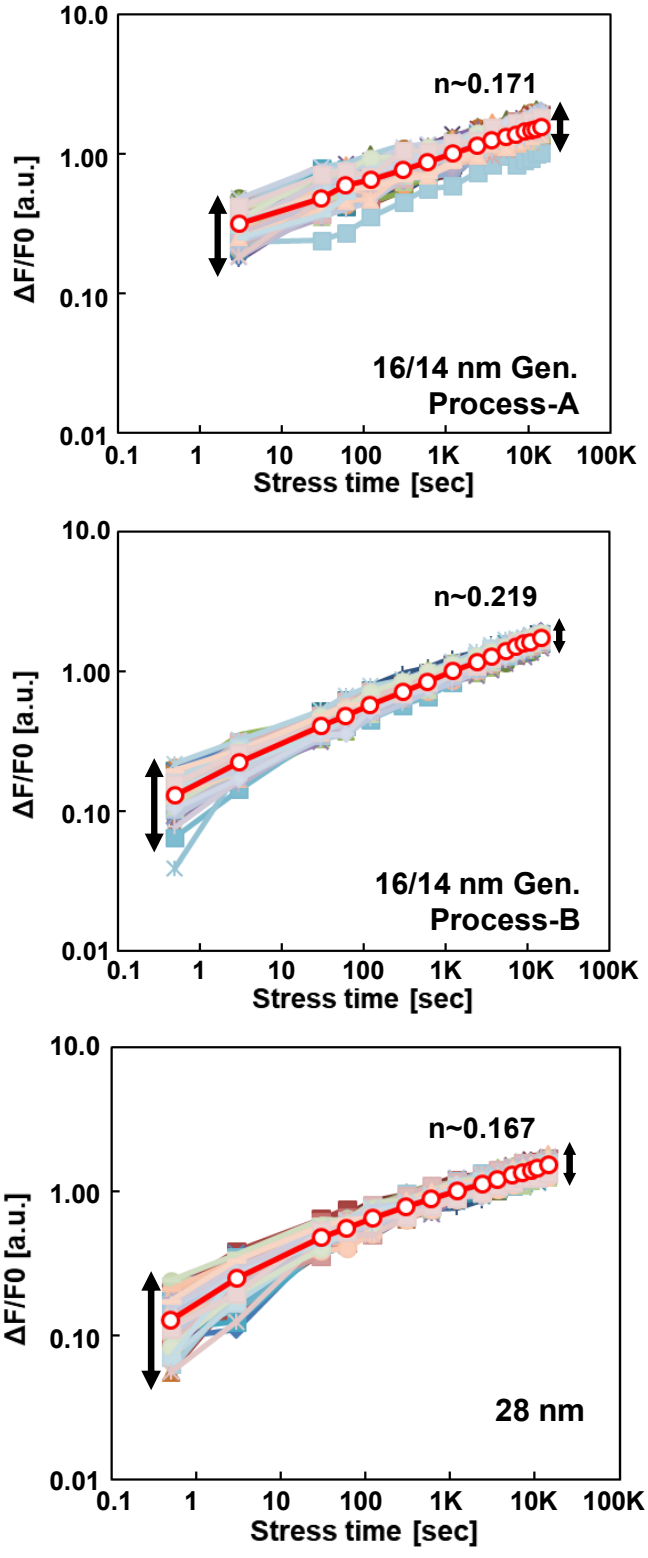


Figure 3.10 Stress time vs. oscillation frequency degradation of 16/14 nm Gen. Process-A, B and 28 nm planar

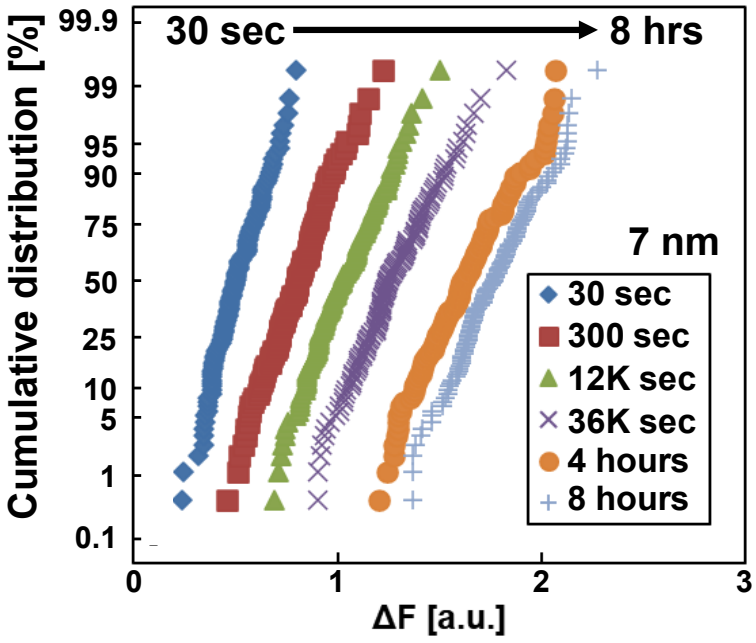


Figure 3.11 Distribution of oscillation frequency degradation by local NBTI variation

Figure 3.12 shows relationship between the standard deviation of ΔV_{thp} ($\sigma(\Delta V_{thp})$) and $\mu(\Delta V_{thp})$ for each stress time and V_{th} flavor. The dots are measurement results, and the solid line is an approximate line when $\sigma(\Delta V_{thp})$ is proportional to the square root of $\mu(\Delta V_{thp})$. As stress time increases, $\mu(\Delta V_{thp})$ increases whereas the ratio of $\sigma(\Delta V_{thp})$ per $\mu(\Delta V_{thp})$ decreases as expected in Figures 3.9 and 3.10, and the measurement results agree well with the approximate line. In this way, $\sigma(\Delta V_{thp})$ is proportional to the square root of $\mu(\Delta V_{thp})$ at any stress time and V_{th} flavors. This indicates that the total number of stress induced trapped carriers follows Poisson distribution as described in ref. [43][44] and this relationship is valid for all stress time and V_{th} flavors. In addition, Figure 3.13 shows measured results of $\sigma(\Delta V_{thp})/\mu(\Delta V_{thp})$ vs. $\mu(\Delta V_{thp})$ of 6 chip results. All of them follow the same universal curve. Furthermore, the measured results of 6 chips of both stress and recovery phases are shown in Figure 3.14 as the black and red shapes, respectively. It shows that recovered ΔV_{thp} also follows the same universal curve. In this way, the amount of local NBTI variation of each V_{th} flavors at various stress and recovery conditions can be estimated by the following simple equation:

$$\sigma(\Delta Vthp) = A \times \mu(\Delta Vthp)^{0.5} \qquad (3\text{-}4)$$

where parameter "A" represents the magnitude of local NBTI variation. As shown in Figure 3.15, the same characteristics is also seen with respect to local BTI variation at the other three processes, where results of 16/14 nm Gen. process-B and the 28 nm planer process include relatively small stress condition (0.5 second).

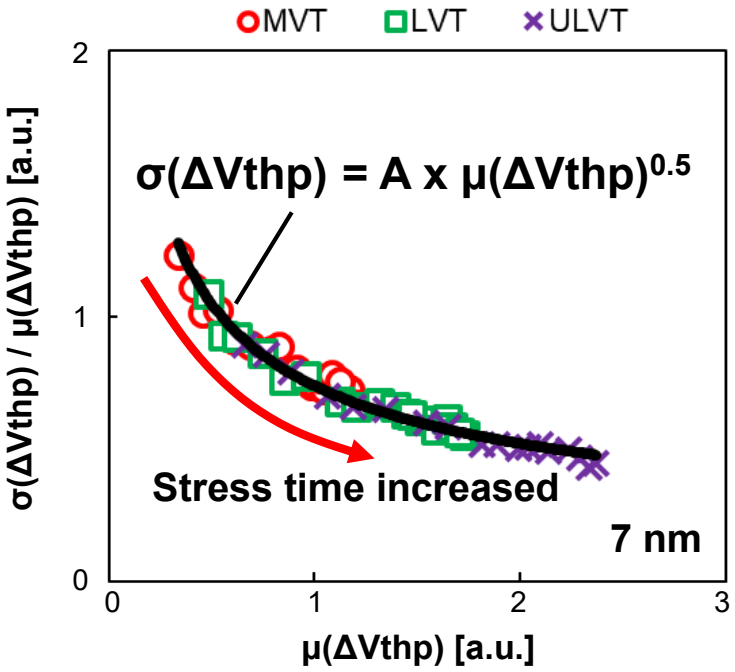


Figure 3.12 Relationship between mean and standard deviation at 3 V_{th} flavors

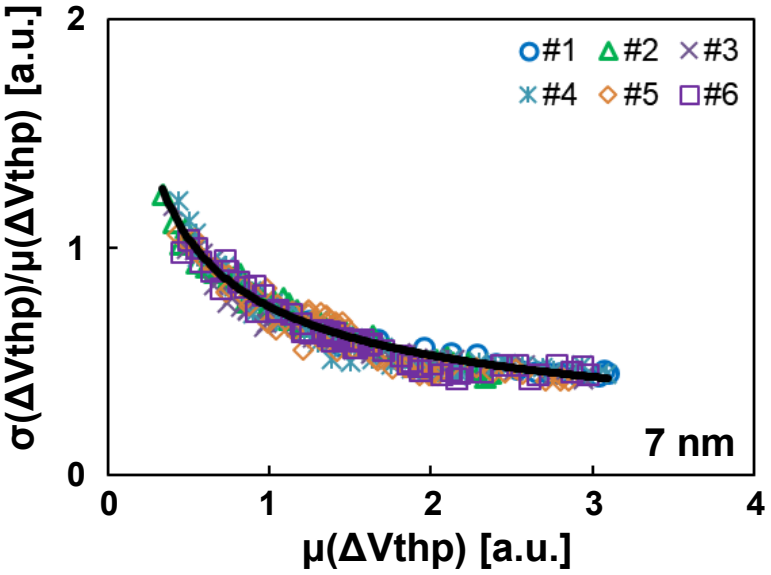


Figure 3.13 σ/μ vs. μ of 6 chip measurement results

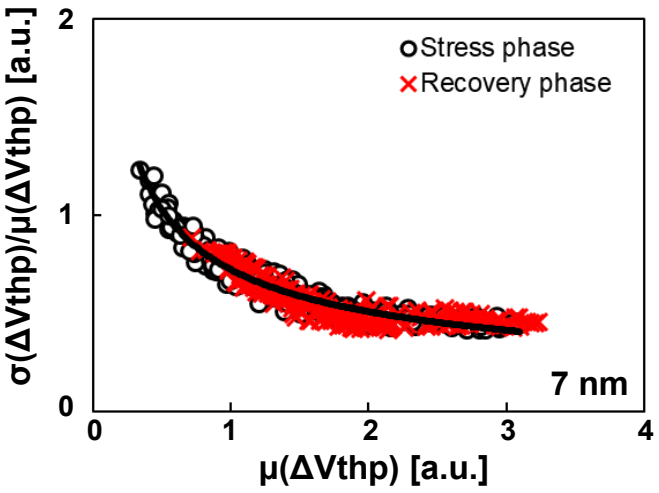


Figure 3.14 σ/μ vs. μ at stress phase and recovery phase

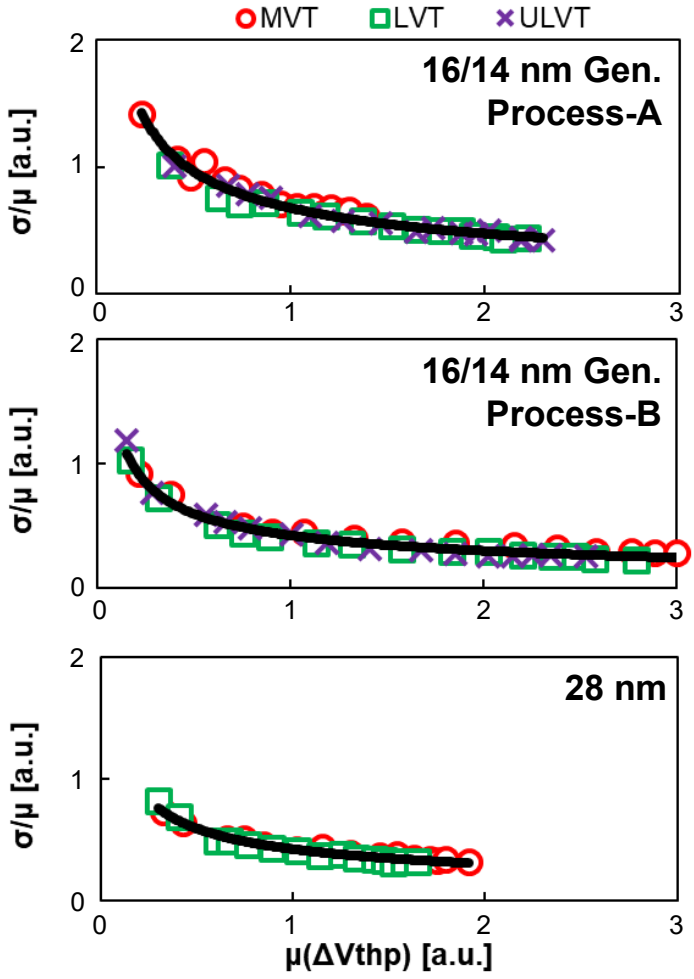


Figure 3.15 σ/μ vs. μ at each process

Figure 3.16 shows the dependence of the number of fins (Fin#) on parameter "A" of the 7 nm FinFET. These were calculated by the measured data of 6 chips in each cell height with Eq. (3-4). Fin# means the number of fins per finger. The parameter "A" becomes 1.4x when Fin# becomes half (from 4 to 2). This rate almost the same as square root of 2. From these results, it is assumed that the magnitude of the BTI induced variation is proportional to the inverse of the root of number of fins in the circuits as same as time-0 variation. In other words, parameter "A" of BTI corresponds to the "Avt" coefficient of process mismatch variation, called the Pelgrom's law [45] shown in following equation

$$\sigma(Vthp) = \frac{A_{VT}}{\sqrt{LW}} \quad (3\text{-}5)$$

where $\sigma(V_{thp})$, L and W mean the standard deviations of threshold voltage due to time-0 variation, gate length and gate width.

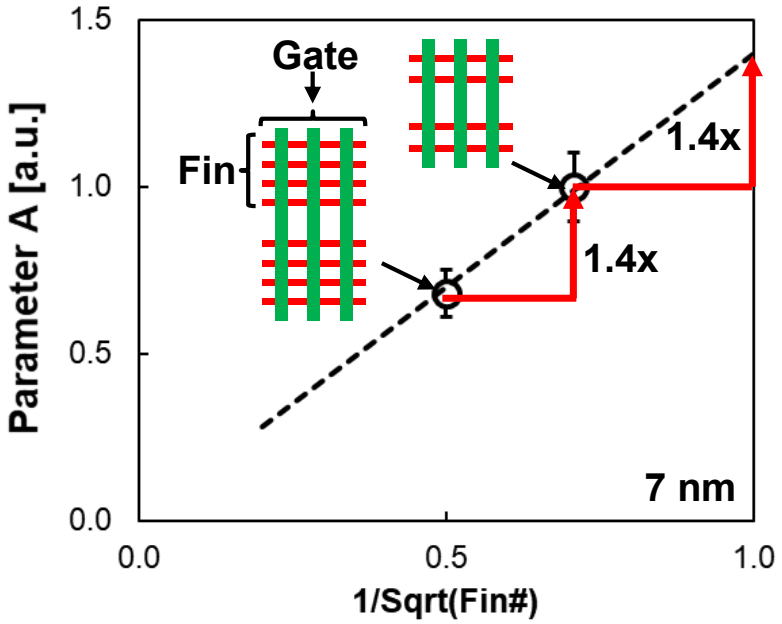


Figure 3.16 Fin number dependency on local NBTI variation factor A

The Parameter "A" of each process is also compared. As for FinFET processes, the parameter "A" with 2 fins is used for comparison based on measurement results or estimation results from other Fin# to make the condition uniform. In case of 28 nm, the standard gate width of the highest density cell library is used. Figure 3.17 shows that the 7 nm FinFET has the largest local BTI variation compared with the 16/14 nm generation FinFET processes and the 28 nm planer process,

and indicates the increase of importance of BTI variability as process technology proceeds.

Figures 3.18 and 3.19 show the correlation between time-0 variation and local NBTI variation. ΔCount at fresh means the difference of the counted number from its mean value before stress. Figure 3.18 shows that the correlation coefficient "R" between time-0 variation and local NBTI variation is 0.014, which can be considered uncorrelated. Figure 3.19 shows its correlation coefficient of each stress time and V_{th} flavor. Since there is almost no correlation between time-0 variation and local NBTI variation at each stress time, these variations are regarded as independent.

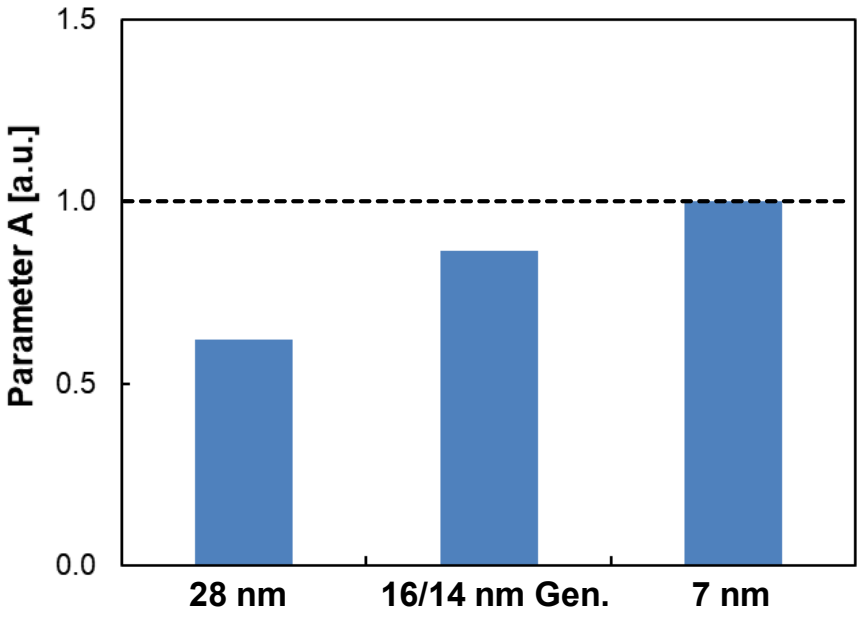


Figure 3.17 Comparison of parameter "A" of each process

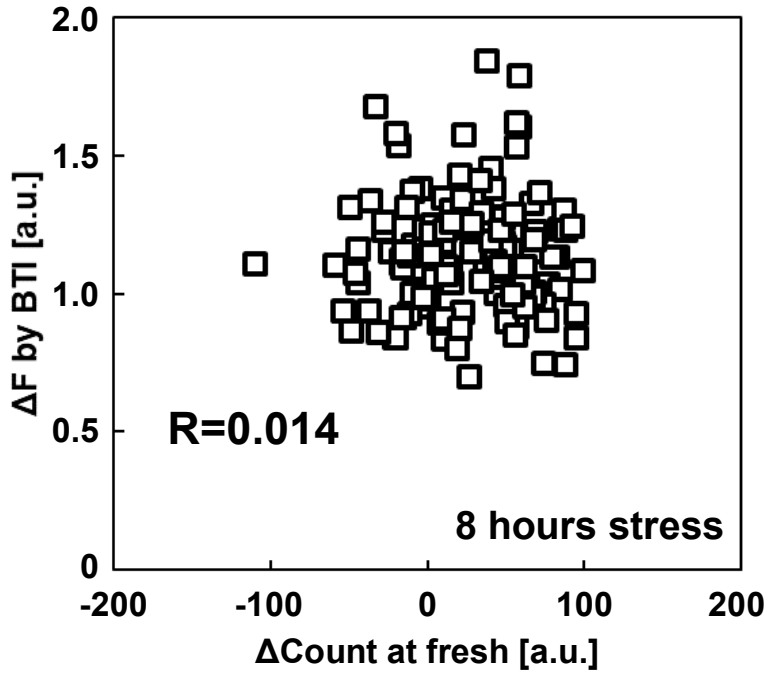


Figure 3.18 Time-0 variation vs. local NBTI variation induced oscillation frequency degradation

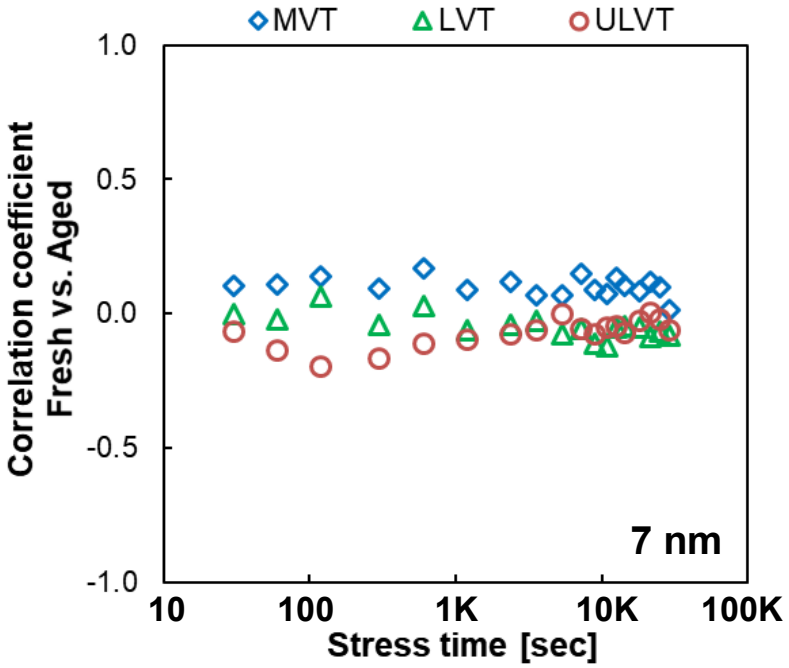


Figure 3.19 Correlation between time-0 variation and local NBTI variation

3.4. Impact of local BTI variation on Logic Circuit and SRAM

In this section, the impact of local NBTI variation on logic circuits and SRAM in the 7 nm FinFET process are discussed.

3.4.1. Analysis of Delay Variable of Logic Circuits

The impact of local NBTI variation on logic circuits is estimated. In this analysis, a specific signal propagation delay affected by NBTI in the normal case, expressed as Tpdlh in Figure 3.20 (a), is focused. Since time-0 variation and local NBTI variation are independent, the total delay variation per stage can be estimated by Eq. (3-6) that treats local NBTI variation follows a normal distribution:

$$\Delta Tpdlh(t) = \sqrt{\left(\Delta Tpdlh_{t0}{}^{2} + \Delta Tpdlh_{NBTI}(t)^{2}\right)} \quad (3\text{-}6)$$

where $\Delta Tpdlh(t)$, $\Delta Tpdlh_{t0}$ and $\Delta Tpdlh_{nbti}(t)$ mean total, time-0 and local NBTI variation for fall input delay, respectively. Since $\Delta Tpdlh_{t0}$ is a time-independent variation factor, it is constant during product lifetime whereas $\Delta Tpdlh_{NBTI}(t)$ is a time-dependent factor following Eq. (3-4) and the sensitivity coefficient of *Tpdlh* to ΔV_{thp} as shown in Figure 3.20(b). As a result, when $\mu(\Delta V_{thp})$ of ULVT becomes 50mV, $\Delta Tpdlh(t)$ of ULVT is 1.11x increased in total by local NBTI variation without considering local BTI. However, as shown in Figure 3.4 and the red line of Figure 3.20(c), there is V_{th} flavor dependency on NBTI and MVT has 2.1x smaller $\mu(\Delta V_{thp})$ than ULVT. This indicate that the impact of local NBTI variation on MVT cell, which has the largest impact of V_{th} variation on its delay because of the smallest *Vov*, can be relaxed. As a result, the uplift of $\Delta Tpdlh$ of MVT is relaxed from 1.11x to 1.06x with considering V_{th} dependency on NBTI.

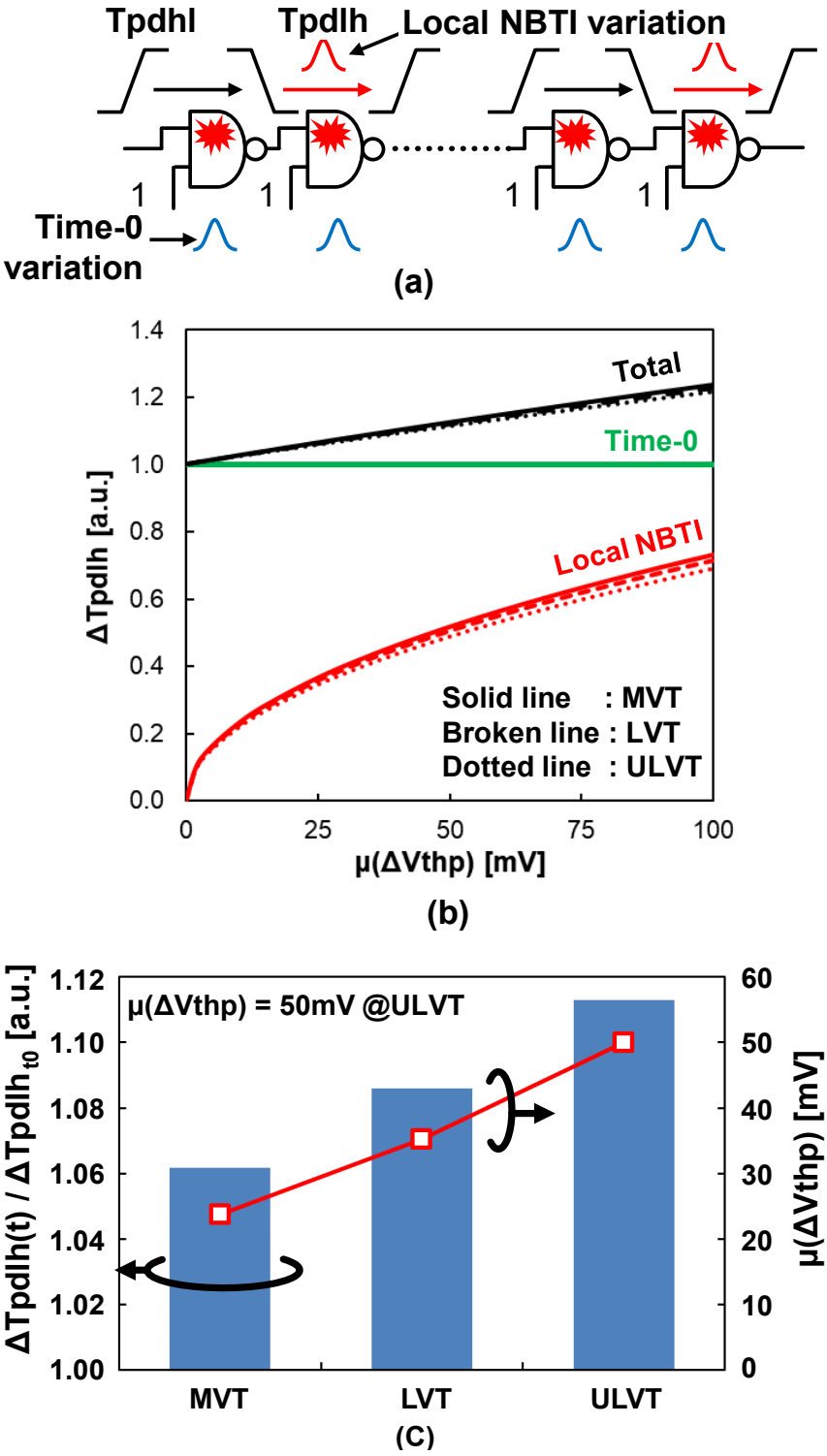


Figure 3.20 (a) benchmark logic circuit, (b) impact of time-0, local NBTI and total variation on logic circuit based on measurement data and simulation (c) The impact of local BTI on circuit delay with considering V_{th} dependency of NBTI at the same stress condition

3.4.2. Analysis of Minimum Operation Voltage of SRAM

How the local NBTI affects SRAM characteristics in 7 nm generation and beyond is examined. In general, a single SRAM bit-cell has its own read/write margin depending on mean V_{th} and its local variation of the 6 transistors inside a bit-cell. Higher PMOS V_{th} degrades SRAM read margin (static noise margin, SNM) while it improves write margin, which indicates that NBTI with PMOS V_{th}-shift induces SNM degradation [46][47]. The characteristic of a single bit-cell inside a SRAM macro manifests itself as the minimum operation voltage, V_{min}. Note that V_{min} is defined as the VDD where the first failure bit appears by lowering cell-array VDD. Figure 3.21 is a simulated fail-bit rate of a single 6T SRAM cell versus VDD without local NBTI before stress ($\mu(\Delta V_{thp})$ =0). The lower the VDD gets, the higher the fail-bit counts become (the smaller the absolute value of σ becomes), and V_{min} is defined at 6σ [31]. A commercial SRAM bit cell's SPICE model is used and sensitivity analysis methodology is shown in [48]. How V_{min} behaves by introducing NBTI mean shift, $\mu(\Delta V_{thp})$ is demonstrated. The detail V_{min} difference between with and without local NBTI ($\sigma(\Delta V_{thp})$) is summarized in Figure 3.22, indicating non-negligible V_{min} degradation due to local NBTI. When $\mu(\Delta V_{thp})$ becomes 100 mV, $\Delta Vmin$ considering local NBTI variation is 1.4x bigger than without local NBTI variation.

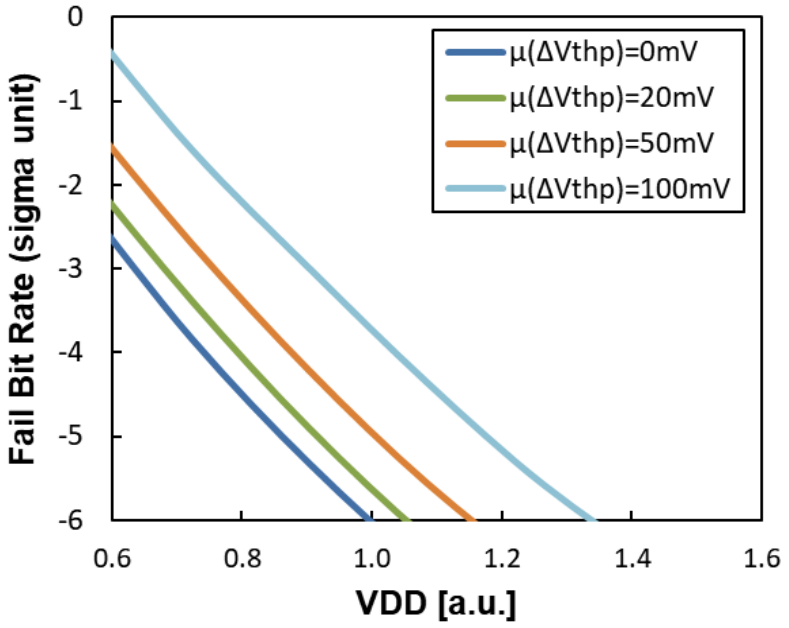


Figure 3.21 Simulated SRAM fail-bit rate vs. VDD without local NBTI variation

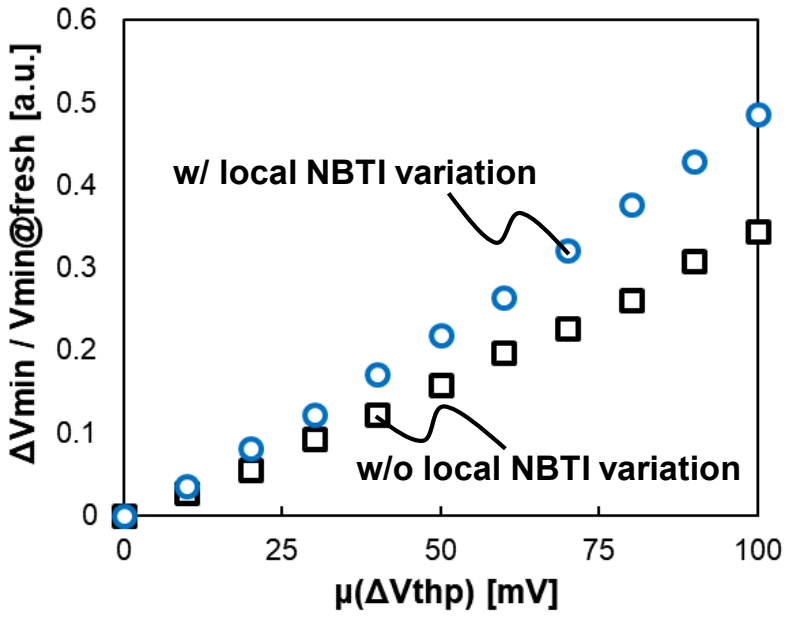


Figure 3.22 Analysis of local NBTI variation induced SRAM Vmin degradation

3.5. Summary

The analysis of BTI degradation of both chip mean BTI and local BTI variation has been presented based on measurement results of Ring-Oscillators (ROs) on TEGs fabricated in a 7 nm FinFET process, two 16/14 nm generation FinFET processes and a 28 nm planer process. The chip mean BTI degradation shows significant V_{th} dependency at the 7 nm FinFET process. The negligibly small PBTI degradation compared with NBTI is also observed at all four processes. As for the analysis of local BTI variation, the standard deviation of NBTI V_{th} degradation is proportional to the square root of the mean value ($\mu(\Delta V_{thp})$) at any stress time, V_{th} flavors and any recovery time in all four processes. The impact of the number of fins and time-0 variation on local BTI are also demonstrated. In addition, when comparing the magnitude of local NBTI variation of each process, it increased as process technology proceeds. From these evaluation results, the impact of local NBTI variation on the characteristics of both logic circuits and SRAM in the 7 nm FinFET are demonstrated. In logic circuits, when NBTI induced V_{th} degradation is 50 mV at ULVT and V_{th} dependency of NBTI is considered, the delay variation of MVT is increased by 1.06x from fresh one due to local NBTI variation. As for the impact on SRAM V_{min}, a simulation result indicates non-negligible V_{min} degradation due to local NBTI variation.

Chapter 4 Highly-Sensitive and Fully-Digital On-Chip Aging Monitor

In this chapter, on-chip NBTI, PBTI and HCI monitors by using standard cell based unbalanced RO are discussed. The monitor consists of NAND and NOR with extremely large difference in drive strength, which enables high sensitivity to BTI compared with a normal Inverter (INV) based RO. In addition, it allows to monitor either one of NBTI or PBTI selectively by making use of the Miller effect caused by the size combination of NOR and NAND. In the HCI monitor, HCI degradation is emphasized by emulating worst-case waveform of logic circuits by using unbalanced drive strength configuration of INV cell. The measurement result of the test chip fabricated in a 28 nm High-k Metal-Gate (HKMG) planer CMOS process and the 7 nm FinFET process are also described.

4.1. Introduction

An annual mileage of cars is expected to be increased in the autonomous driving era since a paradigm shift occurs in terms of cars usage such as car-sharing, ridesharing and so on. The dynamic voltage and frequency scaling (DVFS) technique is often used to optimize power efficiency at each operation scene and to get higher performance by a voltage boost. However, the voltage boost leads to aging degradation such as BTI and HCI. The increase of aging degradation leads to increase guard-band (GB) and restricts the performance. PBTI caused by HKMG process also restricts the performance. As a result, reliability design becomes more severe by both process scaling and car usage change.

It is known that NBTI and PBTI impact are dependent on circuit configurations [31][49]. Therefore, the aging monitor system, which is easy to implement in products with features of high sensitivity and NBTI/PBTI/HCI separations, could be a solution to optimize required GB [50]. In addition, these features help GB optimization and BTI outlier detection at a time of testing before shipment; there are not only process variation but also aging variation between chip-chip, wafer-wafer and lot-lot. However, since a stress on the Burn-In (BI) test which is applied for early defect rejection is effectively small compared to that at the end of life, the normal INV based RO is not enough to detect BTI variation due to small BTI sensitivity. In this way, highly-sensitive and NBTI/PBTI-separated BTI monitors are required. Note that there is another approach to predict

lifetime in a field by environmental parameters (voltage and temperature) with and without any dedicated monitor [51][52][53]. From the point of view of functional safety, combinational usage of any direct monitoring of reliability and in-direct prediction could be a redundant system.

This chapter is organized as followings. Section 4.2 introduces characteristics of highly sensitive aging monitor circuits. Section 4.2.1 and 4.2.2 show basic concept of RO for BTI and HCI monitors. Section 4.2.3 introduces additional proposal for improving BTI sensitivity. Section 4.3 describes the measurement results of test chips to confirm basic characteristics of aging monitors. Brief summary is described in section 4.4

4.2. Highly Sensitive Aging Monitor Circuits

4.2.1. Basic Concept of BTI Monitor Circuit

Figure 4.1 shows comparison of schematic views between the proposed BTI monitor and conventional one. Several RO-based BTI monitors have been proposed [50][54][55][56][57][58] [59][60]. The standard configuration of RO is INV based (INV-RO) [54][55][56][57]. As shown in Figure 4.1 (b), INV-RO with the path gate (PG) can apply NBTI stress only on main INVs during stress period and operate main INVs during oscillation period [58]. In this case, the impact of only NBTI stress can be observed and have 2 times large NBTI impact on the oscillation frequency compared with INV-RO. It is because in case of INV-RO, half of INVs have NBTI stress and others have PBTI stress during DC stress whereas all main INVs have NBTI stress in Type-A. The combination of INV and NOR was also proposed to enhance NBTI sensitivity [50] as shown in figure 4.1 (c). In type-B, NBTI sensitivity can be enhanced because of the stacked PMOS structure of NOR gates. As for the proposed RO, there are two types; one is NBTI sensitive RO (NBTI-RO) and the other is PBTI sensitive RO (PBTI-RO.) The NBTI-RO consists of NOR with the smallest drive strength and the highest PMOS stack count whereas NAND with the largest drive strength in standard cell libraries and all input pins of each NOR and NAND are shorted. Note that these NOR and NAND cells are normally included in a set of standard cell libraries, which realizes easy implementation without any complicated design, high process portability for various process technology nodes and short design Turn-around-Time (TAT). The PBTI-RO is reverse configuration of the NBTI-RO. The GB optimization by defining a critical path replica has been

proposed [61]. However, since there are several critical paths with different NBTI/PBTI sensitivity in an actual design, the critical path replica defined above might not be enough to track actual path's degradation.

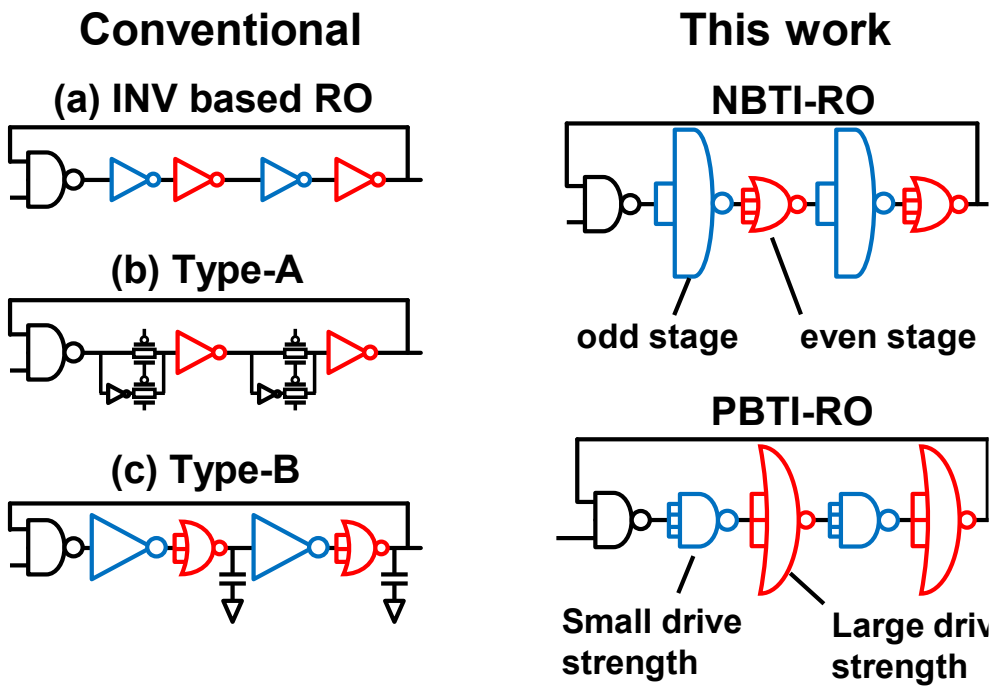


Figure 4.1 Topology comparison between proposed and conventional ROs

Figure 4.2 depicts delay balance and NBTI/PBTI impact of each RO topology under non-oscillation at a time of stress period (DC stress). Those are estimated by SPICE simulations for the 28 nm HKMG planer process. tpdhl_1, tpdlh_1 mean delays at rise and fall input signal of the odd stage cell respectively while tpdhl_2 and tpdlh_2 are those of even stage cells respectively. The delay is normalized by cycle time of each RO. In the case of INV-RO, since each delay is balanced and the input pins at even and odd stages are high and low levels under DC stress, around 25 % of the total delay is affected by NBTI and PBTI, respectively. In the case of ref. [58] shown in Type-A, since each input pin becomes low by PG control, around 50 % of the total delay is affected by NBTI. This means 2x NBTI sensitivity compared to INV-RO. In ref. [50] shown in Typd-B, the fall input delay of NOR becomes large because of weak drivability of the stacked PMOS, resulting in around 2x NBTI sensitivity. Note that this estimation is carefully done to reproduce the result of ref. [50]. Compared with these results, the proposed ROs have the largest delay ratio of tpdlh_2 in NBTI-RO and tpdhl_1 in PBTI-RO, which results in 2.8x and 2.5x sensitivity compared to INV-

RO in term of delay balance. These NBTI-RO and PBTI-RO results are caused by combination of unbalanced drive strength, and small drive strength of NOR and NAND usage for the stacked PMOS and NMOS, respectively.

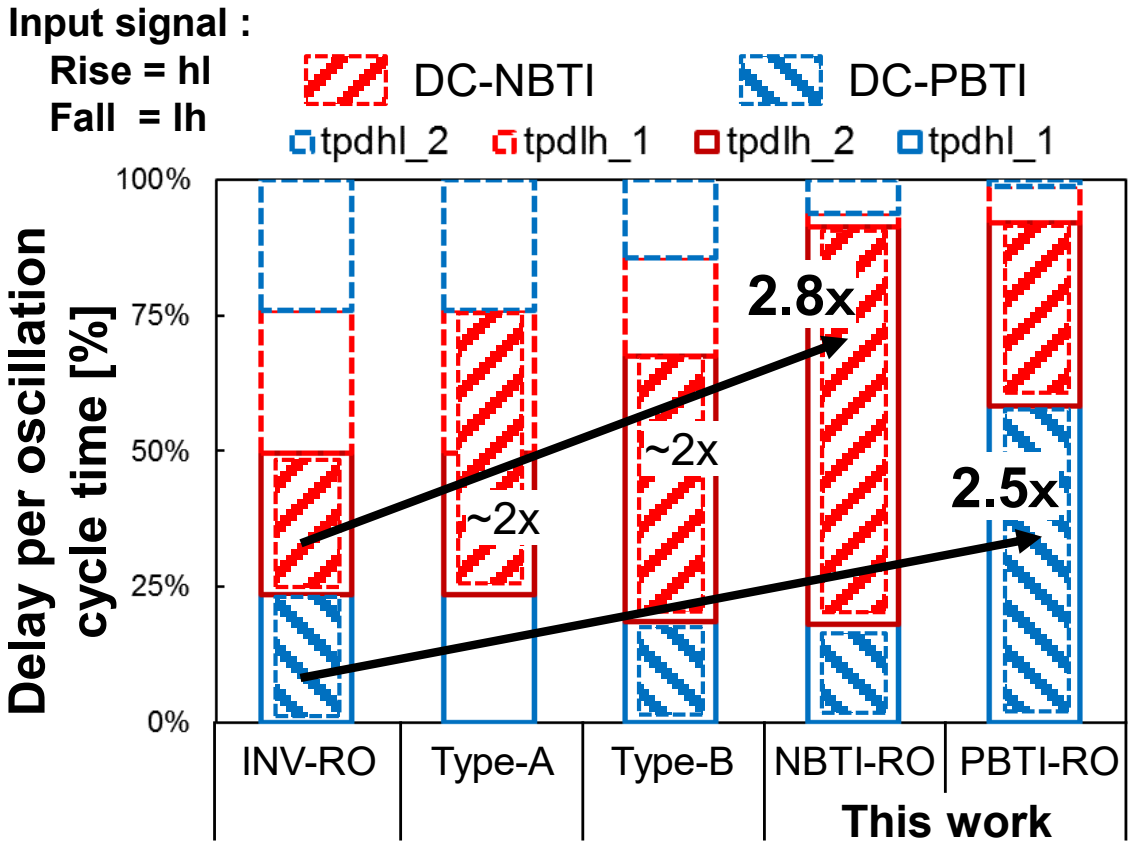


Figure 4.2 Delay components and NBTI/PBTI impact under DC stress

Figure 4.3 demonstrates comparison of NBTI sensitivity with large output transition between INV and NOR cells. In the case of INV, the gate-source voltage (V_{gs}) of the PMOS, which is the difference between the input node and power supply VDD, immediately rises to VDD when the input becomes low and its transition is much smaller than the output transition. On the other hand, in the case of NOR, Vgs2 of the stacked PMOS which is close to the output becomes small during transition of the output node as shown in Figure 4.3. Since small (V_{gs} - V_{th}) makes V_{th} degradation influential on delay (Tpd), the sensitivity of NOR to NBTI increases with increasing output transition. Here V_{th} is the threshold voltage of the PMOS. This operation waveform of input and

output nodes are very close to NOR of NBTI-RO. As a result, the NBTI-RO can achieve higher NBTI sensitivity than expected merely from the dominant delay of NBTI-suffered NOR explained in Figure 4.2. The similar effect can be obtained on PBTI sensitivity at rise input propagation of NAND in PBTI-RO. Note that the gradual rise output of NOR suffered from NBTI further degrades the next-stage NAND delay and thus the NBTI impact is further enhanced.

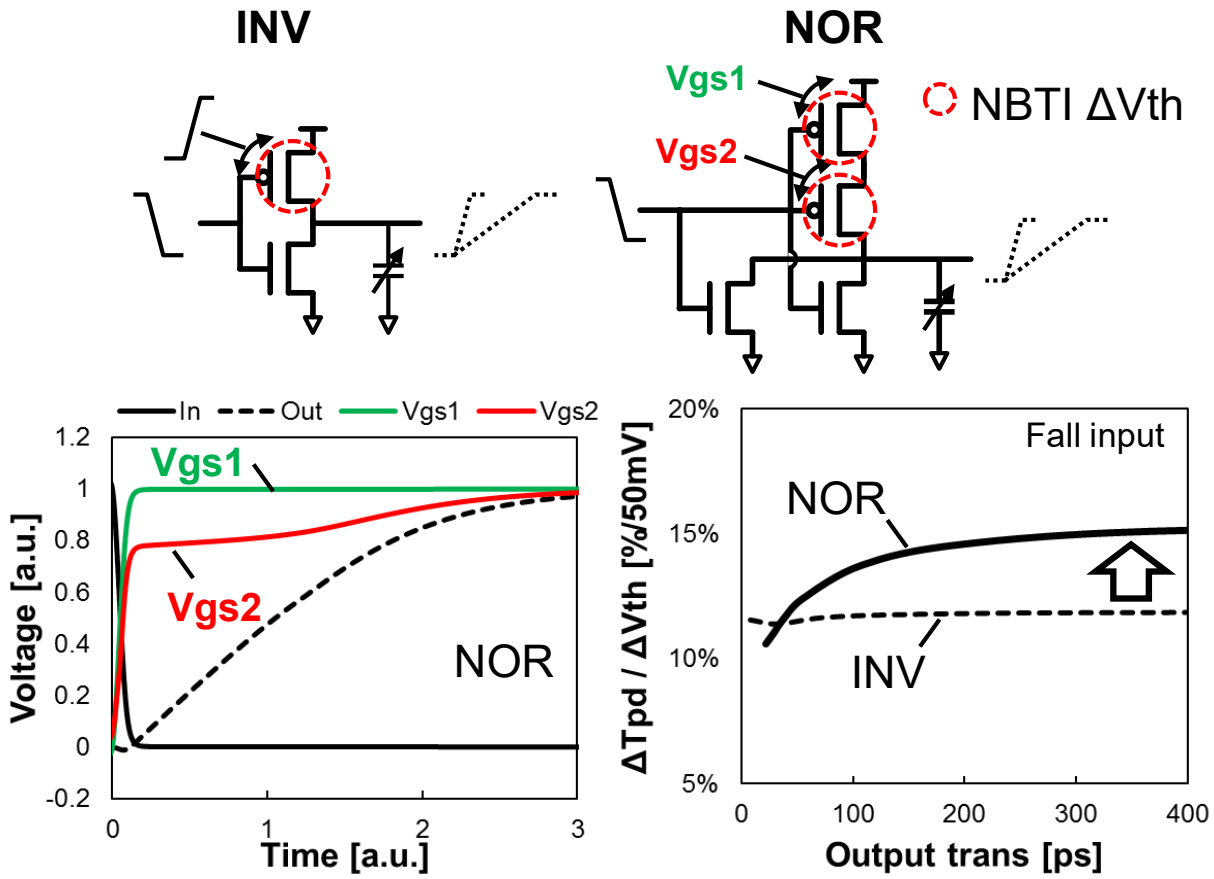


Figure 4.3 NBTI sensitivity improvement by small input and large output transition of NOR

Figure 4.4 compares fresh and aged waveforms of NBTI-RO from SPICE simulations when the fall input signal propagates to NOR. The dotted line indicates the fresh waveform while the solid line indicates PBTI stressed one. In this analysis, PBTI stress on NAND is only considered whereas NBTI stress on NOR is not. The output transition of NOR becomes slow because of large capacitance of NAND whereas that of NAND becomes fast because of its large drive strength. In such case, a large Miller effect occurs during transient period of NAND. As a result, the input signal of NAND becomes substantially flat during its transition period of the NAND output. In other

words, the amount of this constant V_{gs} of NAND NMOS is dominant factor for rise input delay of this NAND. When NAND has PBTI stress, the level of its constant V_{gs} of NAND input due to the Miller effect is increased as shown in the solid line of Figure 4.4. Then the Miller effect compensates the PBTI impact on the NAND delay by pulling up its input voltage during transition. The pulling-up originates from the increased logical threshold triggering the NAND output transition. The increase of logical threshold of NAND at rise input case is due to drivability decrease of NMOS in NAND. In this way, the influence of PBTI degradation is attenuated by the Miller effect, enabling low PBTI sensitivity on NBTI-RO.

Figure 4.5 shows estimation results of NBTI and PBTI sensitivity of the proposed monitors and references under both DC and AC stress. These values are normalized by INV-RO. The NBTI and PBTI sensitivities mean the ratios of delay degradation (ΔTpd) over threshold voltage degradation (ΔV_{th}) for PMOS and NMOS, respectively. AC stress means that RO is oscillating during stress period. In case of AC stress, all active NMOS and PMOS of all cells basically suffer from PBTI and NBTI stress since those transistors alternately turn ON and OFF during oscillation. Comparing the NBTI sensitivity at DC stress, Type-A [58] and Type-B [50] have 2 times NBTI sensitivity, while the proposed NBTI-RO has 4.2 times NBTI sensitivity. The result of Type-A and Type-B can be explained by the difference in the ratio of delay affected by NBTI to the total delay, as shown in Figure 4.2. The highest NBTI sensitivity of NBTI-RO is achieved by a combination of increase of NBTI-affected delay ratios and increase of NBTI sensitivity with the stacked PMOS as explained in Figures 4.2 and 4.3. In NBTI and PBTI separation point of view, Type-B has around 2 times difference between NBTI and PBTI sensitivity while the proposed NBTI-RO and PBTI-RO realize 14x and 17x sensitivity difference. In this way, the proposed BTI monitor, which can be configured with only standard cells, provides the highest BTI sensitivity, NBTI and PBTI separation and ease of implementation in a chip. Thereby, for example, observable 4.2% degradation would occur after Burn-In in case of INV-RO have 1% degradation, which is enough to detect BTI variations and outliers before shipment. In addition, NBTI-RO and PBTI-RO also have 5x sensitivity difference under AC stress although other references generate almost no sensitivity difference. Note that the proposed BTI monitor can suppress HCI influence rather than enhancing [30] and can reduce operation power compared with the case when large drive strength INV is used. This is because the stacked NMOS and PMOS help to reduce voltage stress of HCI and short circuit power during transient time.

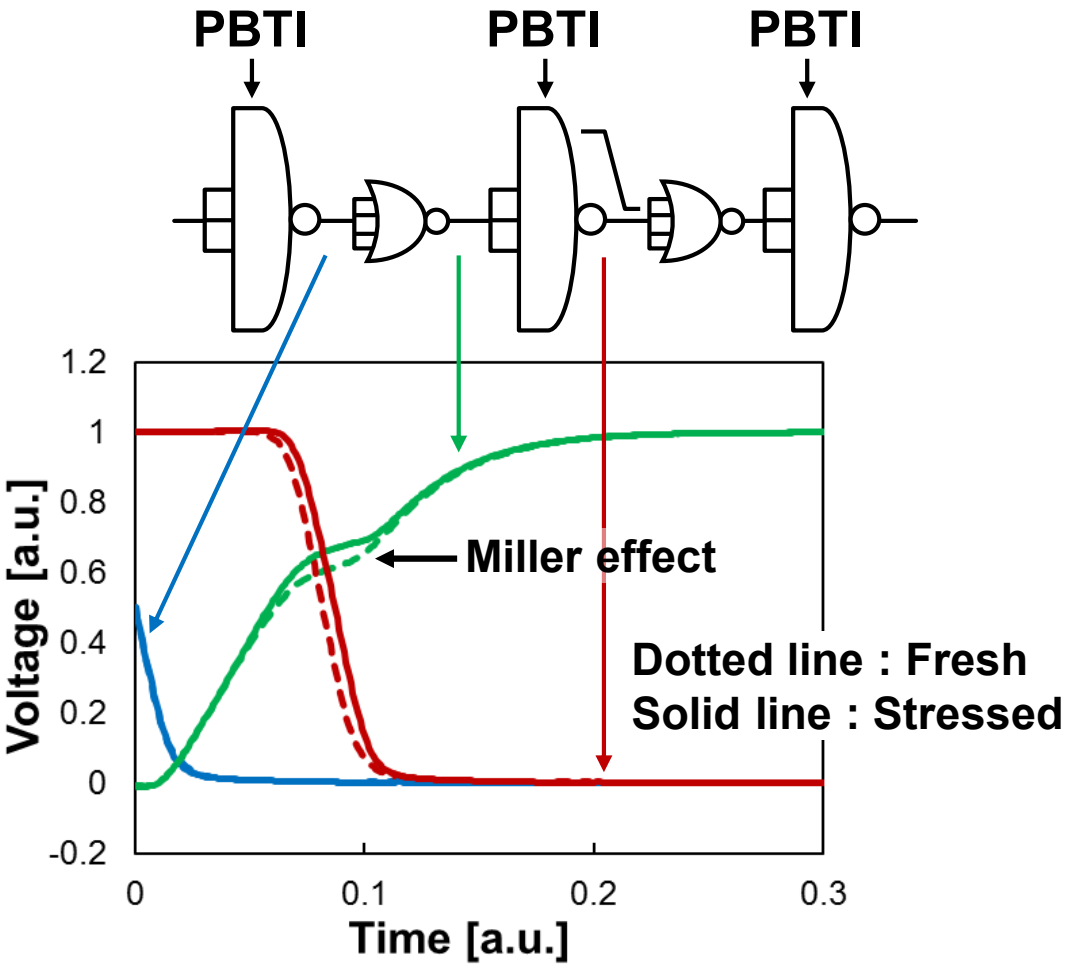


Figure 4.4 Attenuation of PBTI impact on NBTI-RO by Miller effect

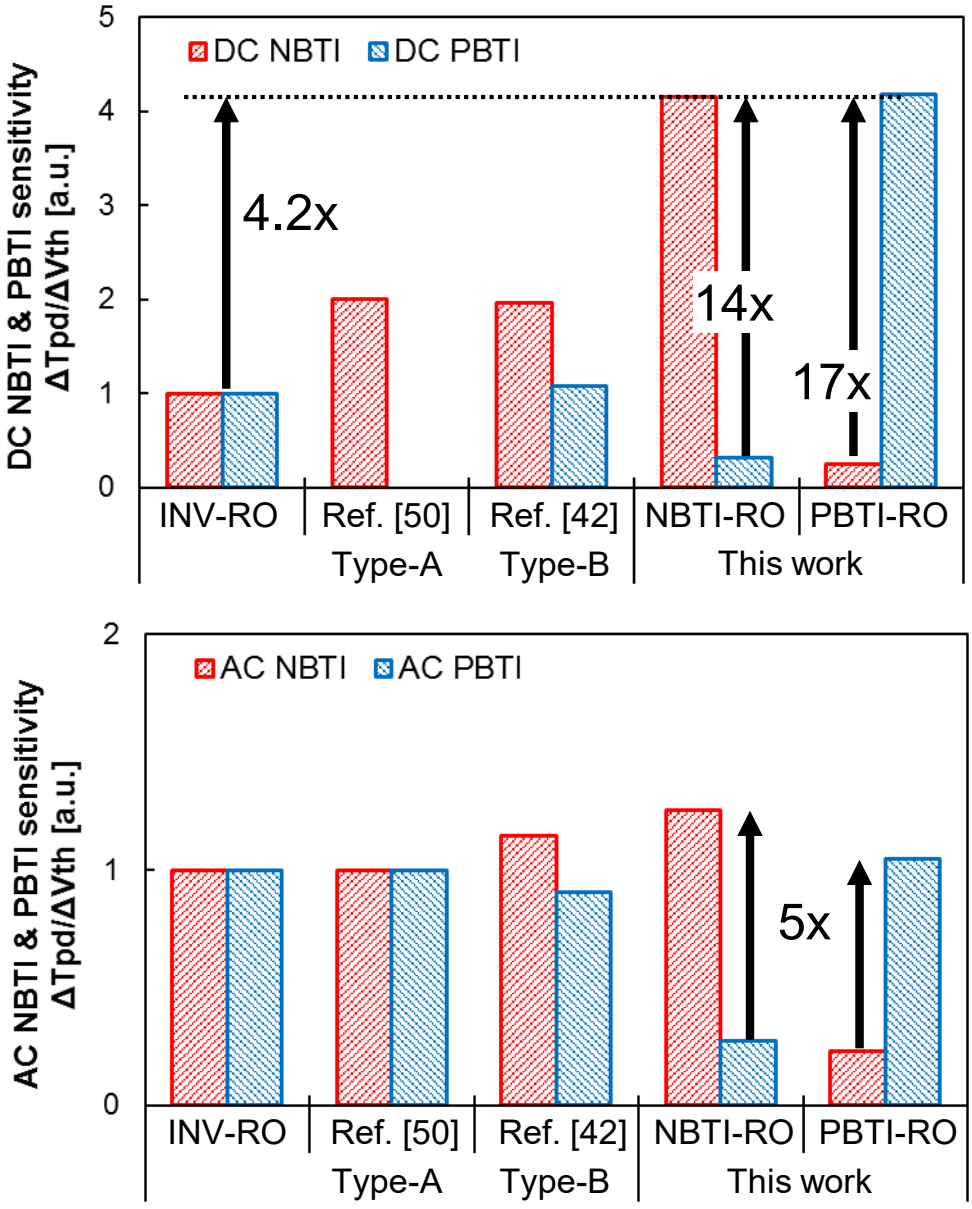


Figure 4.5 Estimated NBTI and PBTI sensitivity comparison under DC stress and AC stress

4.2.2. Concept of HCI Monitor

In logic circuits, HCI degradation occurs only during operation unlike BTI and the impact of HCI strongly depends on the circuit configurations. The operation waveform of small input and large output transition becomes the worst-case operation for HCI degradation in the advanced process technology [30]. It is because larger V_{gs} and drain-source voltage (V_{ds}) lead to cause larger HCI degradation in the scaled process. Figure 4.6 shows topology of highly sensitive HCI RO (ACHCI-RO). ACHCI-RO has a configuration in which INVs of large and small drive strength are connected alternately. A operation waveform of INV with small drive strength in ACHCI-RO simulate small input and large output transition time described above. Figure 4.7 shows transition time per cycle time of product design from statistical timing analysis, the upper limit of design constraint and INV with small drive strength in ACHCI-RO. The transition time of ACHCI-RO is set slightly beyond the product design. In this way, ACHCI-RO simulates the worst HCI degradation operating waveform of the logic circuit. From ref. [30], the cell type used in ACHCI-RO is changed from NAND to INV because the stacked NMOS of NAND decrease V_{ds} at transient time, resulting in reduction of NMOS HCI degradation.

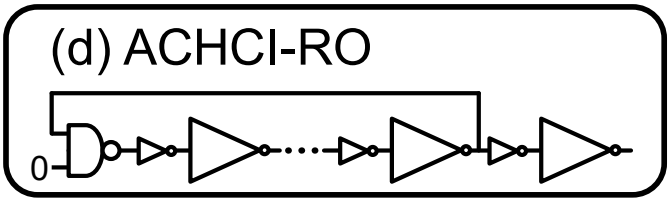


Figure 4.6 Topology of RO for highly sensitive HCI monitor

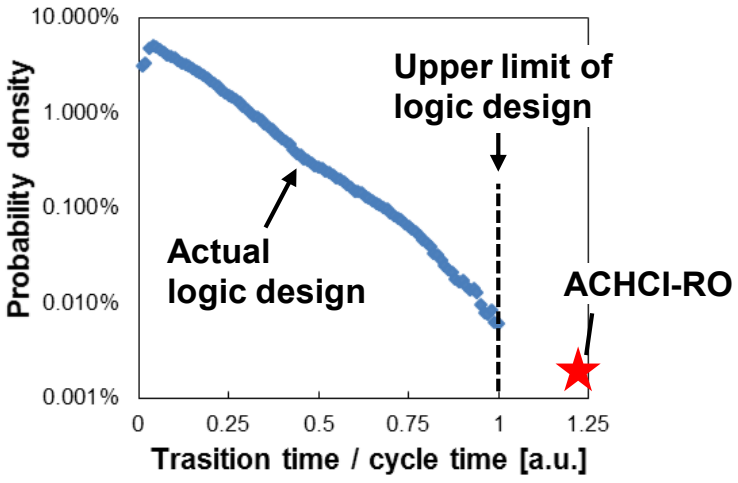


Figure 4.7 Transition time of ACHCI-RO and product design

4.2.3. Enhanced BTI Monitor

Figures 4.8 and 4.9 show comparison of ring-oscillator (RO) topology and BTI sensitivity under DC stress at the 7 nm FinFET process. The circuit diagram of Figure 4.8 shows a state of 0 or 1 of each node when ROs stop oscillation. The red and blue schematics illustrate that each cell has NBTI or PBTI stress during non-oscillation condition, respectively. As shown in Figure 4.8 (a2) and (a3), NAND or NOR based RO can fix all outputs to high or low respectively that can apply NBTI or PBTI stress only on each RO [34][50] although its NBTI or PBTI sensitivity is almost same as that of INV-RO. As shown in Figure 4.8 (a4), the combination of NAND and NOR enhances NBTI and PBTI sensitivity [50] although it has almost the same NBTI and PBTI sensitivity. In contrast, as described in chapter 4.2.1, NBTI-RO shown in Figure 4.8 (b1) has 4.2x NBTI sensitivity. As for R-NBTI-RO and R-PBTI-RO which is the reverse configuration of NBTI-RO and PBTI-RO to invert input voltage of each NAND and NOR cell under DC stress, oscillation frequency is increased after BTI stress despite the NMOS and PMOS performance itself are degraded due to PBTI and NBTI. When the parallel PMOS is degraded by NBTI and the stacked NMOS is not in the NAND cell of R-NBTI-RO, rise input delay of NAND with large input transition time is improved by decreasing PMOS drivability, compared with the fresh one. This unique characteristic enables to increase and decrease NBTI and PBTI sensitivity respectively by taking difference of operation frequency shift of NBTI-RO (ΔF1) and R-NBTI-RO (ΔF2). Figure 4.10 shows the proposed NBTI monitor configuration as a representative. “F1” and “F2” mean oscillation frequency of NBTI-RO and R-NBTI-RO at time 0, respectively. “F1_aged” and “F2_aged” mean oscillation frequency of NBTI-RO and R-NBTI-RO after stress, respectively. Since “F0” and “F1” is almost the same, “F0_aged - F1_aged” is almost equal to “ΔF1 - ΔF2”. As a result, the NBTI monitor has 6.2x NBTI sensitivity and negligibly small PBTI impact shown in Figure 4.11(a). In addition, the influence of temperature variation on ΔF can be compensated to multiply ΔF by the temperature dependent table (T-table), which is determined by information collected from the on-chip temperature sensor. As shown in Figure 4.11(b), simulation result shows the error rate of this temperature correction is less than 4% in various process and voltage conditions. Table 4.1 summarizes the aging monitor comparison.

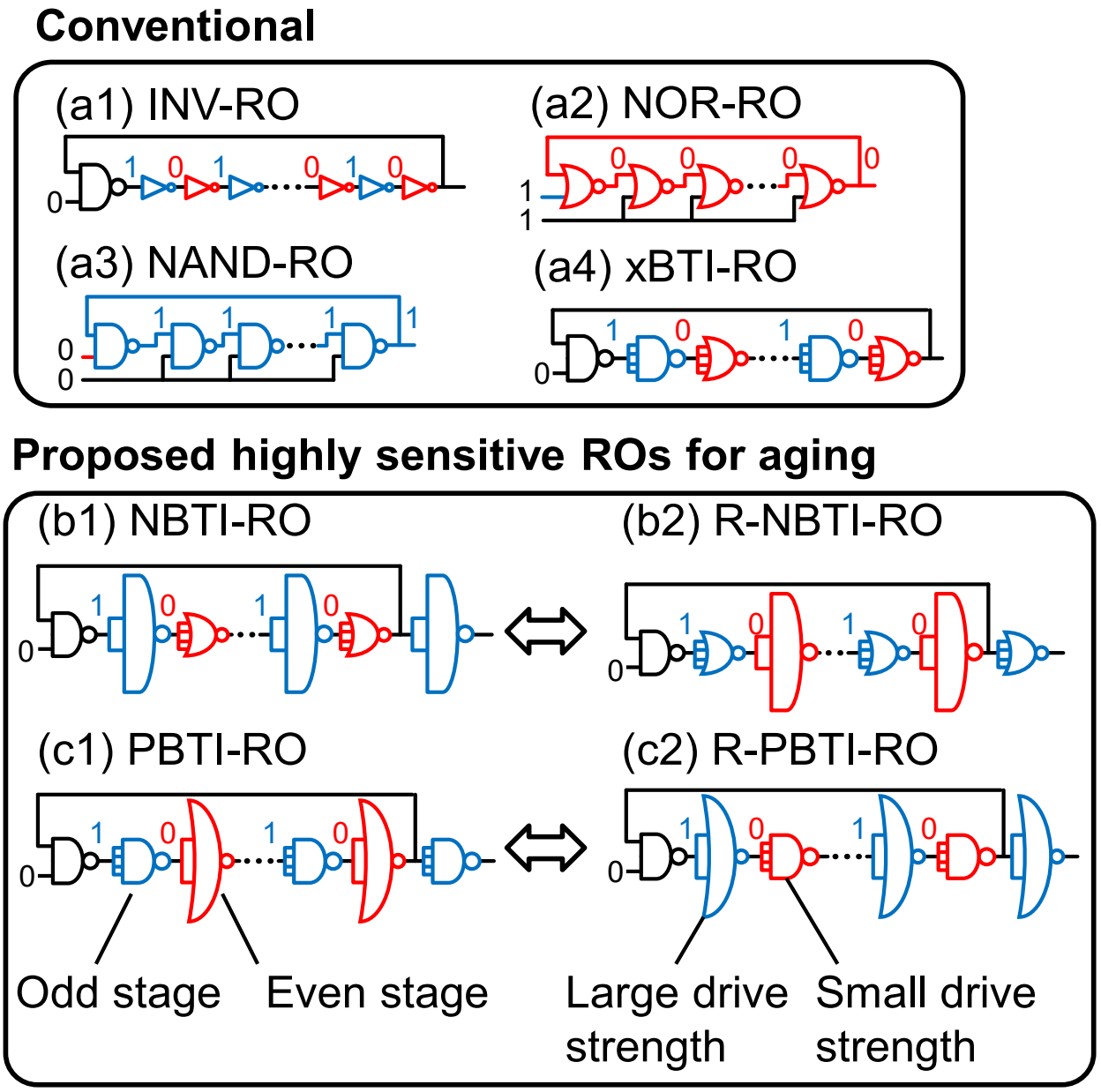


Figure 4.8 Topology of conventional ROs and improved highly sensitive ROs for aging

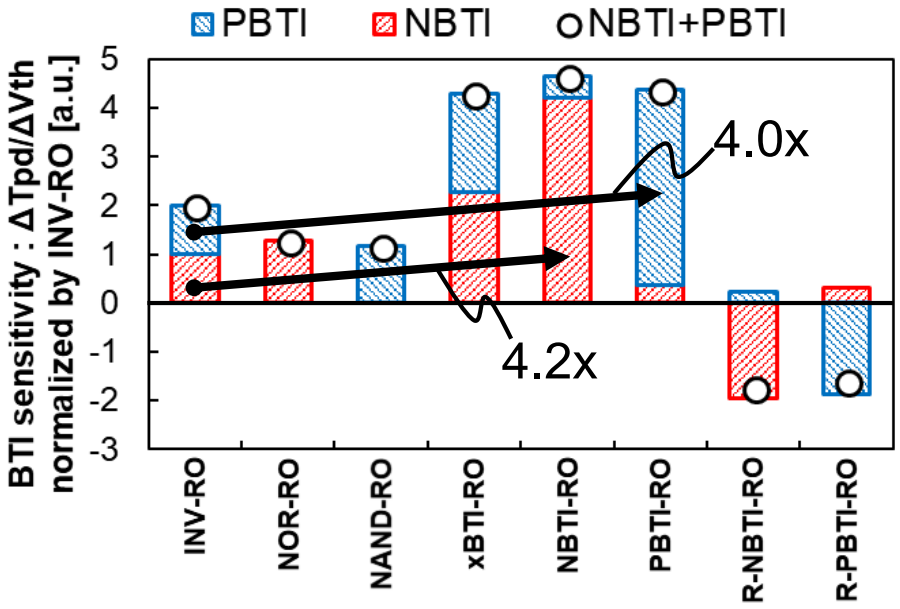


Figure 4.9 Simulated NBTI and PBTI sensitivity at 7 nm FinFET process

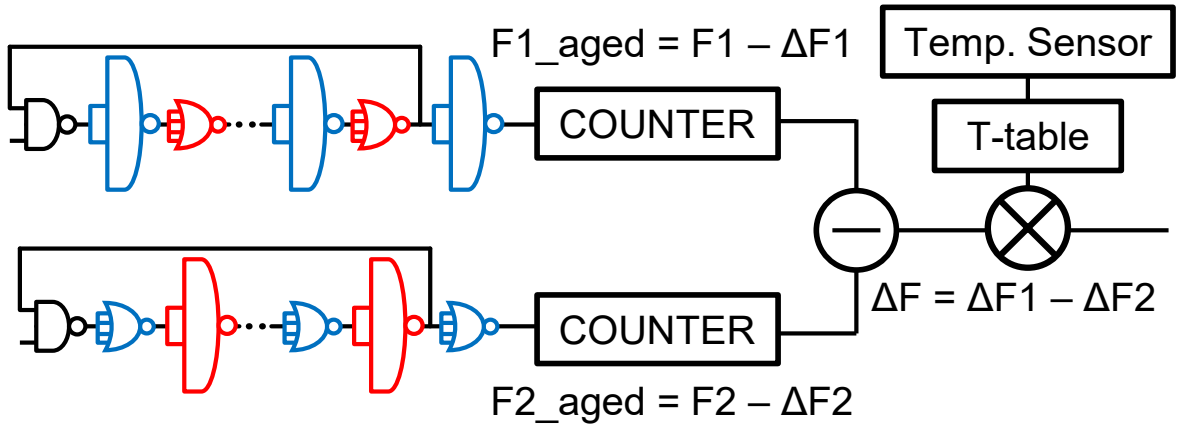


Figure 4.10 Proposed NBTI-monitor configuration

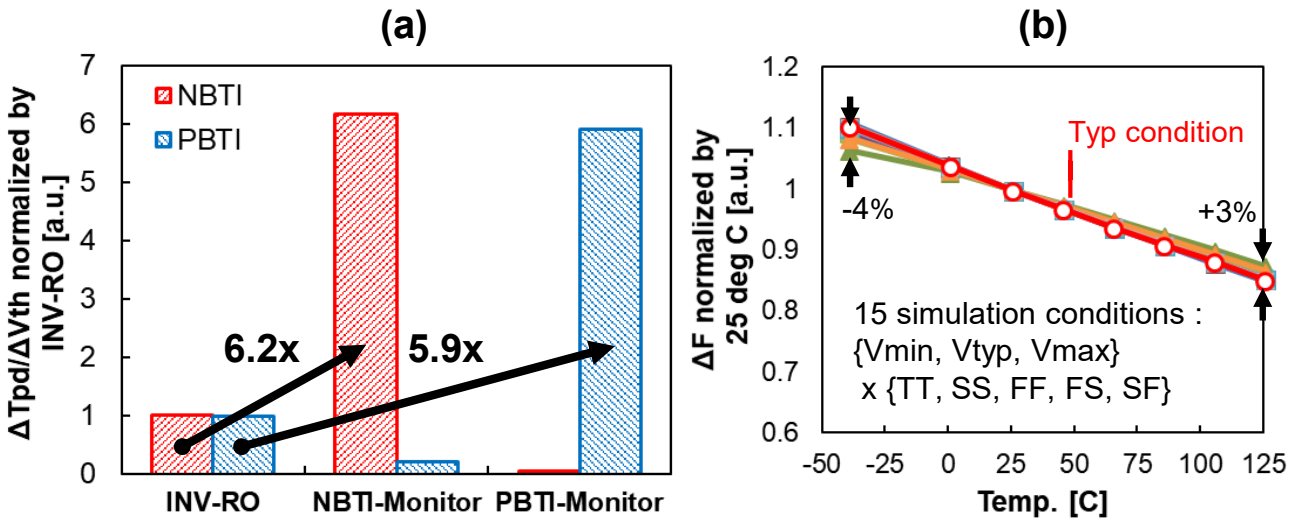
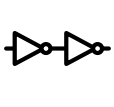
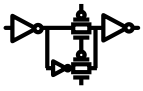
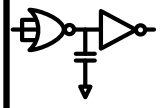
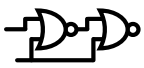
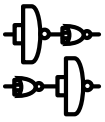
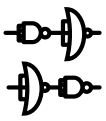
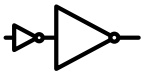


Figure 4.11 Characteristics of proposed NBTI/PBTI-monitor. (a) NBTI/PBTI-Monitor sensitivity, (b) Temperature dependency

Table 4.1 Comparison of BTI monitor

	INV-RO	IRPS 2015	IRPS 2013		This work		
Diagram of monitor Circuit							
BTI sensitivity @DC stress	1x	~2x	~2x	~1.3x	**6.2x** @NBTI	**5.9x** @PBTI	~1x
NBTI & PBTI Separation	No	Yes	No	Yes	**Yes** (~28x diff.)	**Yes** (~100x diff.)	No
AC-HCI stress enhancement	No (1x)	No (1x)	No (< 1x)	No (< 1x)	No (< 1x)	No (< 1x)	**Yes** (3.6x)
Imple-mentation	Std. cell Only	Path Gate Needed	Std. cell only		**Std. cell only**		

4.3. Test Chip Evaluations

4.3.1. Measurement Results in 28 nm HKMG process

A test chip was in the 28nm HKMG planer process to confirm the characteristics of NBTI-RO and PBTI-RO. Figure 4.12 shows a die phot and layout pattern of the test chip. There are three types of ROs, NBTI-RO, PBTI-RO and PBTI-RO with PG, and the number of stages of all ROs is 61. The area of each RO is 138 μm^2, 195 μm^2 and 728 μm^2, respectively. The 2-input NAND-based RO is also implemented as a reference.

Figure 4.13 shows measured result of NBTI-RO, PBTI-RO and reference RO of 5 chips after 9 hours DC stress at 125 degrees. The stress voltage is more than 1.4 times higher than the nominal voltage. V_{th} degradation (ΔV_{th}) of NBTI and PBTI are estimated by the least mean square method from simulated BTI sensitivity $\Delta Tpd/\Delta V_{th}$ and measured ΔTpd based on Eq. (3-1). The median value of estimated ΔV_{th} of 5 chips is shown in Figure 4.13(a). The red and blue bars mean estimated ΔV_{th} of NBTI and PBTI, respectively. PBTI degradation is smaller than NBTI but not negligibly small due to HKMG process [10][11]. Based on these estimated ΔV_{th} of NMOS and PMOS, the components of NBTI and PBTI of each measured ΔTpd are decomposed. Plots are measured ΔTpd, and red and blue bar graphs represent the estimation results of NBTI or PBTI induced Tpd degradation of each RO. The "#1", "#2", "#3", "#4" and "#5" shown in figure 4.13(b) mean chip identification numbers. The measured ΔTpd of 3 ROs are well correlated with the simulation results of sum of red and blue bars even though those ROs have significant sensitivity difference of NBTI and PBTI.

Figure 10 shows measured results of PBTI-RO with PG. This RO has two stress mode, one is “NBTI only” mode and the other is “Mixed” mode to confirm small sensitivity of NBTI in PBTI-RO. NAND and NOR cells have PBTI and NBTI stress respectively in “Mixed” mode at a time of stress period, whereas both NAND and NOR have NBTI stress in “NBTI only” mode by biasing input and output node of both NAND and NOR cells to the low and high level by PG and the 3-state buffer. The simulation result of reference RO with PG at “NBTI only” mode is estimated as a reference. In “Mixed” mode, PBTI-RO with PG shows large PBTI induced Tpd degradation as same as Figure 4.13(b) because of its high PBTI sensitivity. In contrast, the measured result of ΔTpd at “NBTI only” mode is much smaller than that of “Mixed” mode like the simulation result despite the degradation of NBTI is around 45 mV and larger than that of PBTI. In this way, the proposed PBTI-RO can realize the highest sensitivity of PBTI as well as low NBTI sensitivity on its delay.

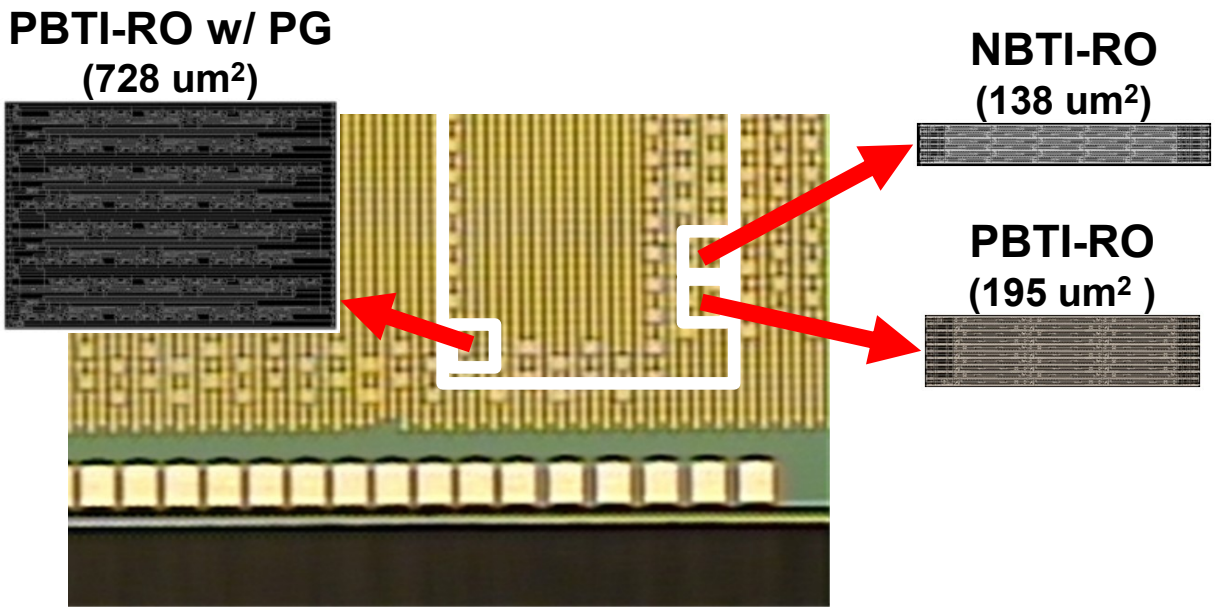


Figure 4.12 Die photo and layout pattern of test chip in 28 nm HKMG

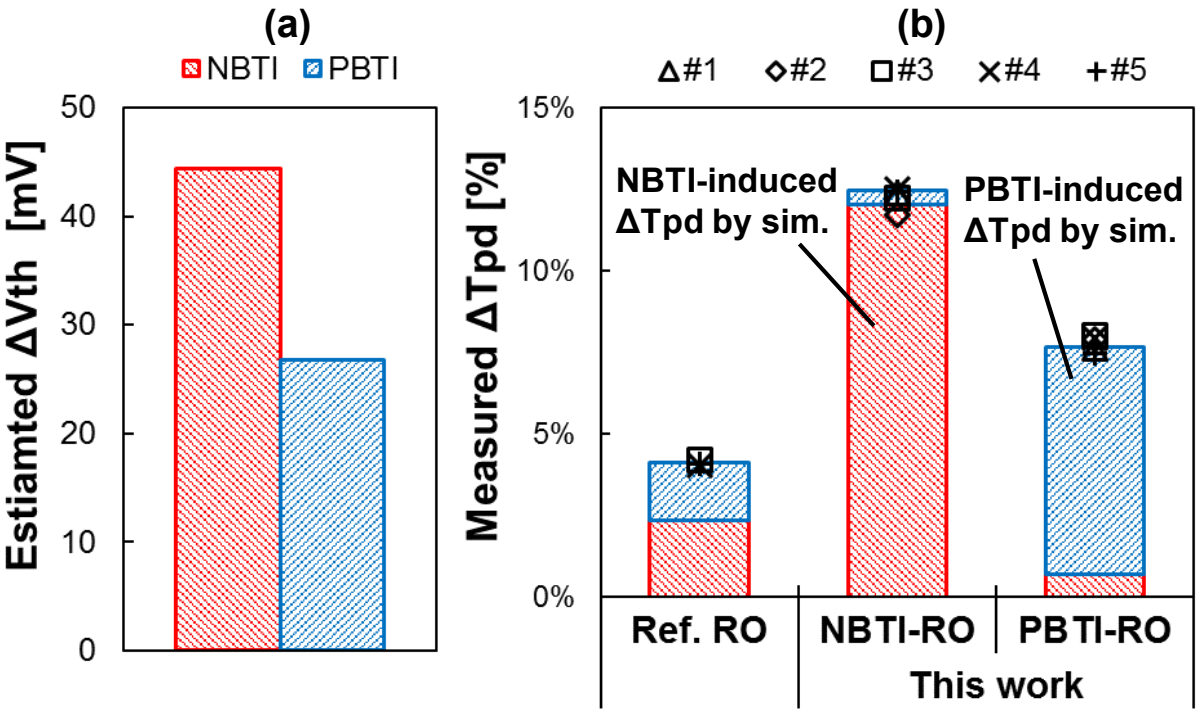


Figure 4.13 Measured result and estimated NBTI/PBTI impact

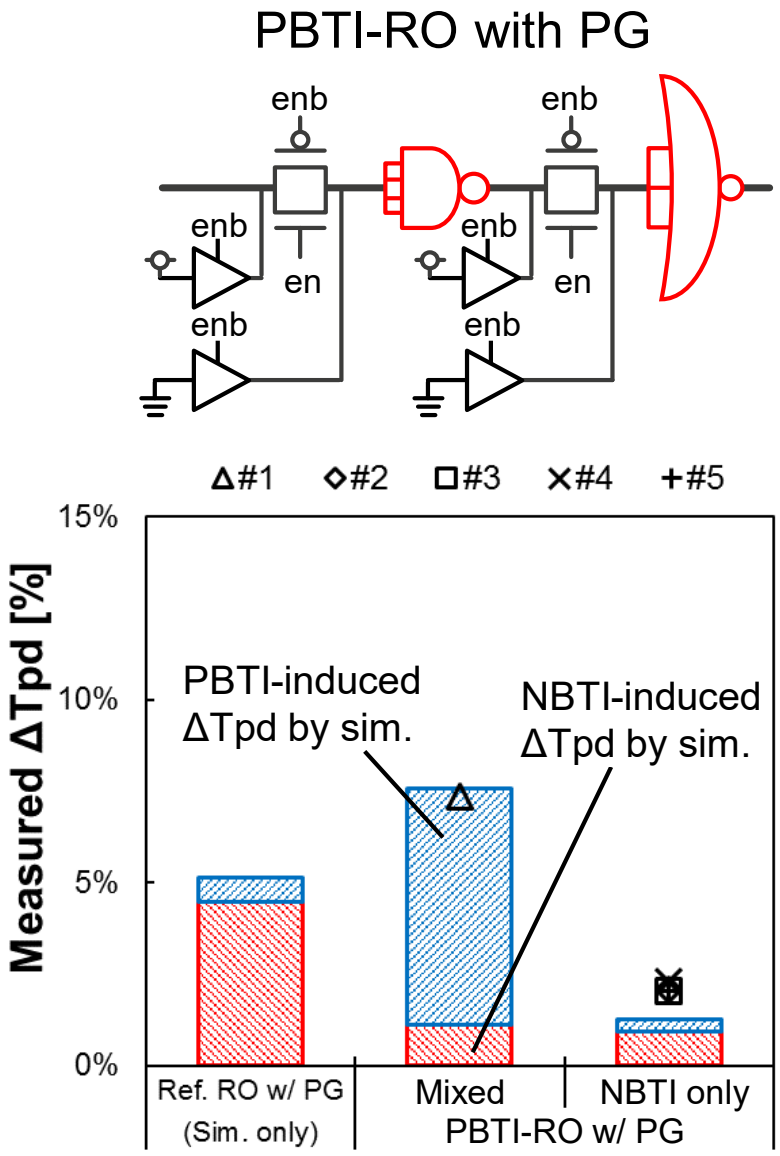


Figure 4.14 Measured result of PBTI-RO with PG for confirmation of small NBTI sensitivity

4.3.2. Measurement Results in 7 nm FinFET Process

A test chip was fabricated in the 7 nm FinFET process to confirm the basic characteristics of each RO. Figure 4.15 shows a die photo and list of ROs implemented in the test chip. 9 types of ROs are implemented. High voltage and high temperature stress are applied. This total amount of stress is intended to cover the expected field stress of the product. Stress voltage is more than 1.5 times higher than the nominal voltage. First, ΔV_{th} of NBTI and PBTI are estimated to multiply the simulated BTI sensitivity of NOR-RO and NAND-RO by the measured delay degradation ΔTpd of them, respectively. It is because NOR-RO and NAND-RO can be selectively applied by NBTI or PBTI stress, respectively. Figure 4.16 shows estimated ΔV_{th} of NBTI and PBTI for both of the 7 nm and 16 nm FinFET process [62]. #1, #2, #3, #4, #5 and #6 mean chip identification numbers. NBTI is the dominant factor for both of the 7 nm and 16 nm compared to PBTI. The main difference between 16 nm and 7 nm is V_{th} type dependency. In 7 nm, the lower V_{th} device obviously provides the worst NBTI, which is similar to ref. [36].

Figure 4.17 shows comparison between measured and estimated ΔTpd of each RO caused by BTI after DC stress. ΔTpd is estimated by using estimated ΔV_{th} shown in Figure 4.16 and simulated NBTI and PBTI sensitivity of each RO. The dotted line means that measured and estimated ΔTpd is exactly matched. It is successfully confirmed that measured and estimated ΔTpd of all RO types are well correlated. Note that measurement result of not only NBTI-RO but also NBTI-RO-R is as expected by simulations. The measured ΔTpd of NBTI-RO-R becomes negative, meaning improvement of its delay. The maximum error rate, defined as ratio of measured data per estimated one, of NBTI monitor is less than 6%. Figure 4.18(a) shows normalized measurement and simulation result of INV-RO and two ACHCI-ROs with different number of stages under AC stress. AC stress means RO is oscillating during stress period. The bar graph shows simulation results, and the circles mean the median values of the measurement result. HCI degradation is only considered in this simulation. HCI degradation is increased by reproducing the worst-case waveform of logic circuits like the difference between INV-RO and ACHCI-RO at same number of stages. It is also increased with decreasing number of stages of RO because a ratio of switching operation time per unit time is increased, results in increase of HCI stress. As a result, 3.6x high HCI sensitivity of ACHCI-RO is estimated compared with INV-RO by simulation. Measurement results of ΔTpd are well explained by this simulation result. Furthermore, as shown in Figure 4.18(b), the recovery effect was not observed as with the characteristics of HCI even if the recovery time, which is the total value of the power-off time, increased. In this way, it is confirmed that the dominant degradation factor of ACHCI-RO is HCI and has 3.6x sensitivity compared with INV-RO.

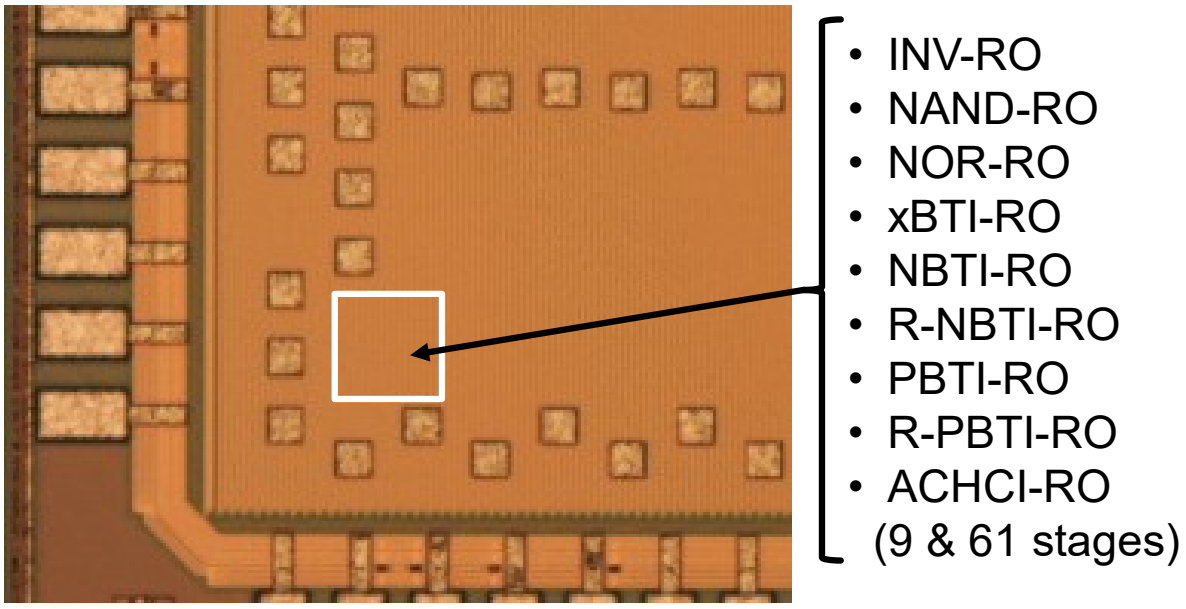


Figure 4.15 Die photo of a test chip in a 7 nm FinFET process

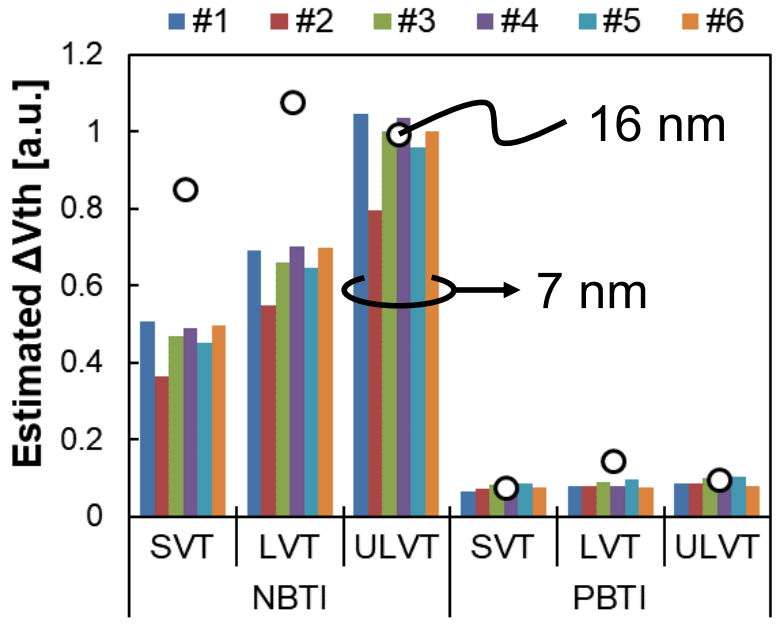


Figure 4.16 ΔV_{th} estimation by NOR-RO and NAND-RO measurement result

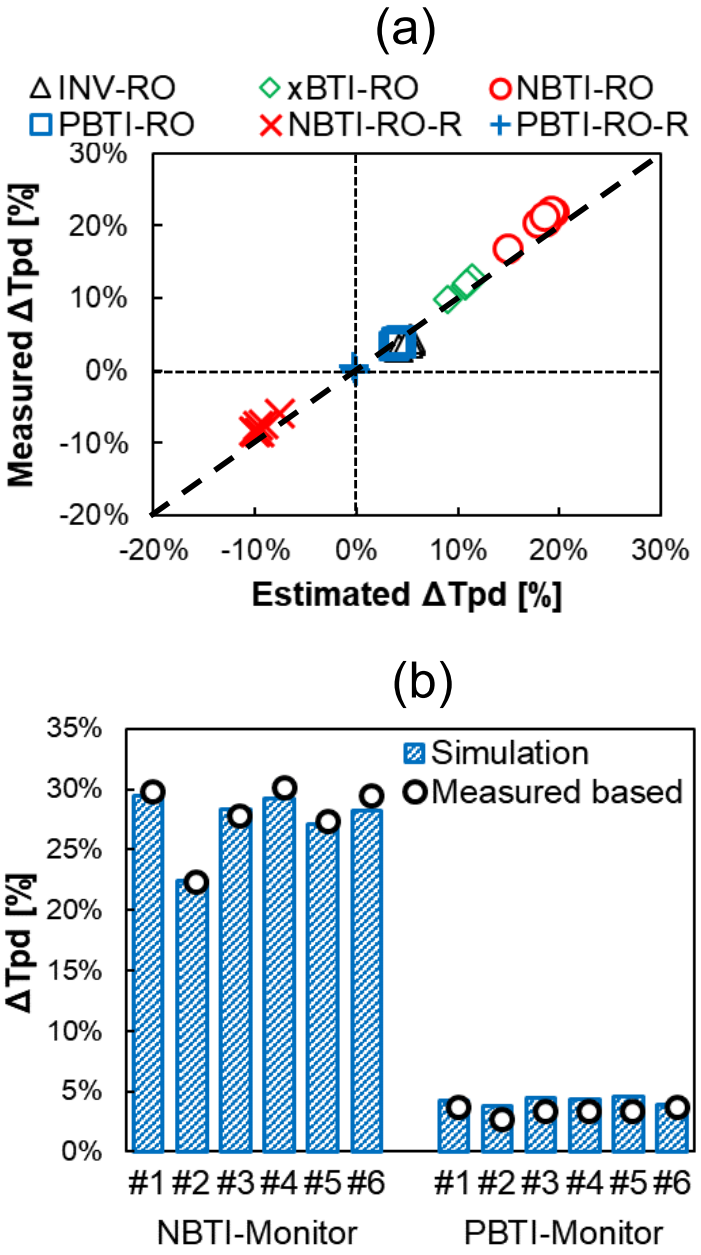


Figure 4.17 Measurement and estimated result under DC stress. (a) Measured result of each RO, (b) NBTI/PBTI-monitor characteristics

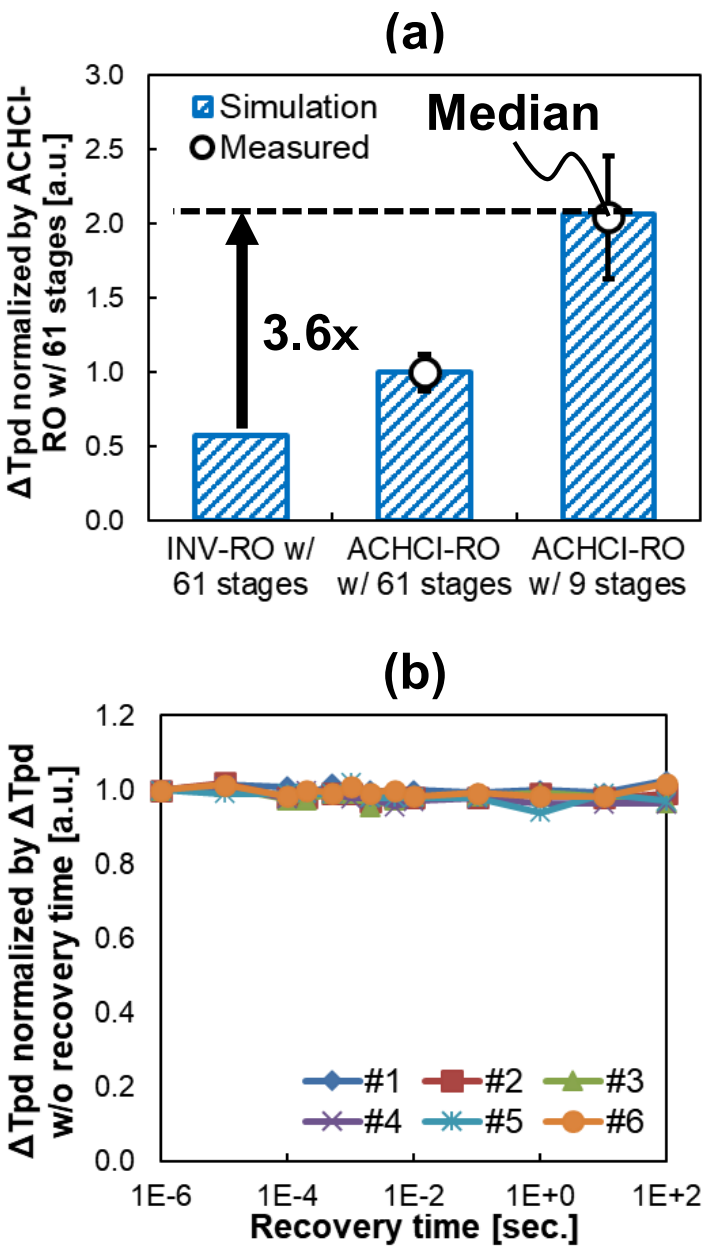


Figure 4.18 Measurement result of ACHCI-RO under AC stress. (a) Measured and HCI simulation result, (b) Recovery effect of ACHCI-RO

4.4. Summary

The on-chip NBTI, PBTI and HCI monitors by using standard cells based unbalanced RO are presented. NBTI sensitive RO (NBTI-RO) and PBTI sensitive RO (PBTI) consist of unbalanced drive strength combination of NAND and NOR cells. The NBTI-RO and PBTI-RO have over 4 times high sensitivity at DC stress compared with the normal INV-based RO. This high sensitivity is caused by the unbalanced delay and ΔV_{th} sensitivity improvement of the stacked MOS by increasing output transition time. The Miller effect caused by large drive strength cells mitigates PBTI influence of NBTI-RO. In addition, R-NBTI-RO, which consists of reverse cell order of NBTI-RO, is used for further increase and decrease of NBTI and PBTI sensitivity for the NBTI monitor, respectively. R-NBTI-RO gets fast after NBTI stress where as other ROs are degraded. As a result, 6.2x NBTI sensitivity compared with the normal INV-RO and negligibly small PBTI sensitivity are achieved in the 7 nm FinFET process. The PBTI monitor is vice versa. In the HCI monitor, HCI degradation is 3.6x emphasized by emulating worst-case waveform of logic circuits by using the unbalanced drive strength configuration of the INV cell. The measurement result of test chips fabricated in the 28 nm HKMG planer process and the 7 nm FinFET process show that measured results of each RO are well matched to the simulation ones. These highly sensitive NBTI/PBTI/HCI monitors could be a solution to optimize required guard-band in a field, detect variations and outliers of aging at time of testing to achieve both high performance and high reliability of LSI.

Chapter 5 Conclusion

In this thesis, the study of BTI variability due to local layout effect (LLE) and statistical BTI variability inside chips in advanced CMOS process technologies are described by measuring ROs for optimal robust design. In addition, highly sensitive on-chip digital aging monitors composed of ROs are described.

In chapter 1, the background of this research area and the purpose of this study are explained. The challenges of design for reliability of integrated circuit (IC) are increasing with the spread of application, demand of high performance and low power, and progress of process scaling. Therefore, the importance of study of BTI induced variability and on-chip aging monitors are increased for satisfying both high performance and high reliability. The characteristics of BTI and HCI and those impacts on logic circuits are briefly described for better understanding of this study.

In chapter 2, the analysis methodology of LLE of BTI by using various ROs with different BTI sensitivities is introduced. The measurement result of the test chip is demonstrated in a 10 nm Fin Field Effect Transistor (FinFET). The LLE impact of BTI's LLE on various standard cell is analyzed by comparing estimated degradation without considering LLE and measured one. In this process, standard cells with large drive strength have relatively small BTI degradation compared with those with small drive strength. The LLE impact on the recovery effect of BTI is also discussed and there is no significant dependency on standard cell type. These impacts can be considered in logic design with the well-known on-chip variation (OCV) methodology.

In chapter 3, the analysis of local BTI variation inside a chip is described based on measurement results of RO fabricated in a 7 nm FinFET process, two 16/14 nm generation FinFET processes and a 28 nm HKMG planer process. The standard deviation of NBTI threshold voltage (V_{th}) degradation is proportional to the square root of the mean value ($\mu(\Delta V_{thp})$) at any stress time, V_{th} flavors and any recovery time in all of the four processes. The impact of number of fins and time-0 variation on local BTI variation are also demonstrated. In addition, when comparing the magnitude of local NBTI variation of each process, it is increased as the process technology proceeds. Based on these evaluation results, the impact of local NBTI variation on the characteristics of both logic circuits and a static random access memory (SRAM) are discussed in the 7 nm FinFET case. As for the impact on SRAM minimum operation voltage (V_{min}), non-negligible V_{min} degradation due to local NBTI variation is demonstrated.

Chapter 4 describes on-chip negative BTI (NBTI), positive BTI (PBTI) and HCI monitors by using standard cell based unbalanced ROs. As for the NBTI sensitive RO (NBTI-RO), it consists

of unbalanced drive strength combination of NAND and NOR cells, realizing over 4 times high sensitivity at DC stress compared with the normal Inverter (INV) based RO. This high sensitivity is caused by the unbalanced delay and ΔV_{th} sensitivity improvement of the stacked MOS with increasing output transition time. The Miller effect caused by large drive strength cells mitigates PBTI influence on NBTI-RO. In addition, R-NBTI-RO, which composed of the reverse cell order of NBTI-RO, is used for further increase and decrease of NBTI and PBTI sensitivity for the NBTI monitor, respectively. As a result, 6.2x NBTI sensitivity compared with the normal INV-RO and negligibly small PBTI sensitivity are achieved in the 7 nm FinFET process. PBTI monitor is vice versa. In the HCI monitor, HCI degradation is 3.6x emphasized by emulating the worst-case of logic circuit by using unbalanced drive strength configuration of the INV cell. The measurement result of test chips fabricated in the 28 nm HKMG planer process and the 7 nm FinFET process are demonstrated and show that the proposed ROs realize the characteristics expected from the SPICE simulation results.

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1) Mitsuhiko Igarashi, Yuuki Uchida, Yoshio Takazawa, Makoto Yabuuchi, Yasumasa Tsukamoto, Koji Shibutani and Kazutoshi Kobayashi, “An Analysis of Local BTI Variation with Ring-Oscillator in Advanced Processes and Its Impact on Logic Circuit and SRAM,” IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences,
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Acknowledgements

I would like to express my gratitude to Professor Kazutoshi Kobayashi of Kyoto Institute of Technology for providing me a great opportunity to study in his laboratory, his detail review and valuable advice for this research. I would like to express my gratitude to Professor Shigetaka Kumashiro, Professor Masahiro Yoshimoto, Professor Yuichi Kado and associate Professor Akira Hiroki of Kyoto Institute of Technology, for their detail review and insightful suggestions. I also would like to express my gratitude to Professor Koji Nii of Kyoto Institute of Technology for his invaluable supports and insightful discussions.

This thesis comprises the results of experiments that have been undertaken at Renesas Electronics Corp. I am exceedingly grateful to the Vice President of Renesas Electronics Corp., Mr. Toshinori Inoshita, Senior Distinguished Engineer of Renesas Electronics Corp., Mr. Hiroyuki Kondo for providing me an opportunity to study as a doctoral student.

I would like to express my enormous appreciation for useful advice and discussions from my colleagues of Renesas Electronics Corp.: Mr. Koji Shibutani, Dr. Yasumasa Tsukamoto, Mr. Yoshio Takazawa, Mr. Hirotoshi Sato, Mr. Kazunori Onozawa, Mr. Masaki Shimada, Mr. Yuuki. Uchida. I am grateful as well to Dr. Makoto Yabuuchi and Dr. Kan Takeuchi.

I would like to express my appreciation to all students in Kobayashi's laboratory for their valuable discussion.

Finally, I would like to express my appreciation to my family for their great supports.