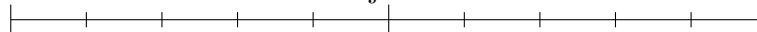


10cm Width. Print it out just in 10cm.



Master's Thesis

Title How to Write a Bachelor
 or Master Thesis in English

Supervisors Prof. Taro Denshi

 Prof. Jiro System

Graduate School of Science and Technology

Department of Electronics

Student ID 00121000

Denko Matsugasaki

Date: Feb. XXth, 20XX

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How to Write a Bachelor or Master Thesis in English

20XX

00121000

Denko Matsugasaki

abstract

How to Write a Bachelor or Master Thesis in English

平成 20XX 年

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松ヶ崎 電子

概要

日本語の概要

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Chapter 1

Introduction

This document explains how to write a bachelor's technical report or a master thesis in department of electronics, Kyoto Institute of Technology by L^AT_EX.

You can download related files from the following URL.

<http://www-vlsi.es.kit.ac.jp/kitesthesis/>

If you have any question or comment, please contact with Prof. Kobayashi (kazu-toshi.kobayashikit.ac.jp).

Chapter 2

My Research

2.1 Sample Figures and Tables

Fig. reffigsample is a sample figure. You can see a sample graph drawn by Gnuplot in Fig. 2.2.

Table 2.1 give a sample table.

You can refer related papers by `\cite{}` L^AT_EXcommand. For example, [1] first proposed the concept of variation-aware reconfiguration. Mr. Tosaka from Fujitsu presented a paper related to soft errors[2]. In COMPEL 2016, Prof. Rivas presented a paper related to SiC MOSFET[3]. [4] generally introduces power electronics.



This is a sample figure.

Figure 2.1: Sample figure.

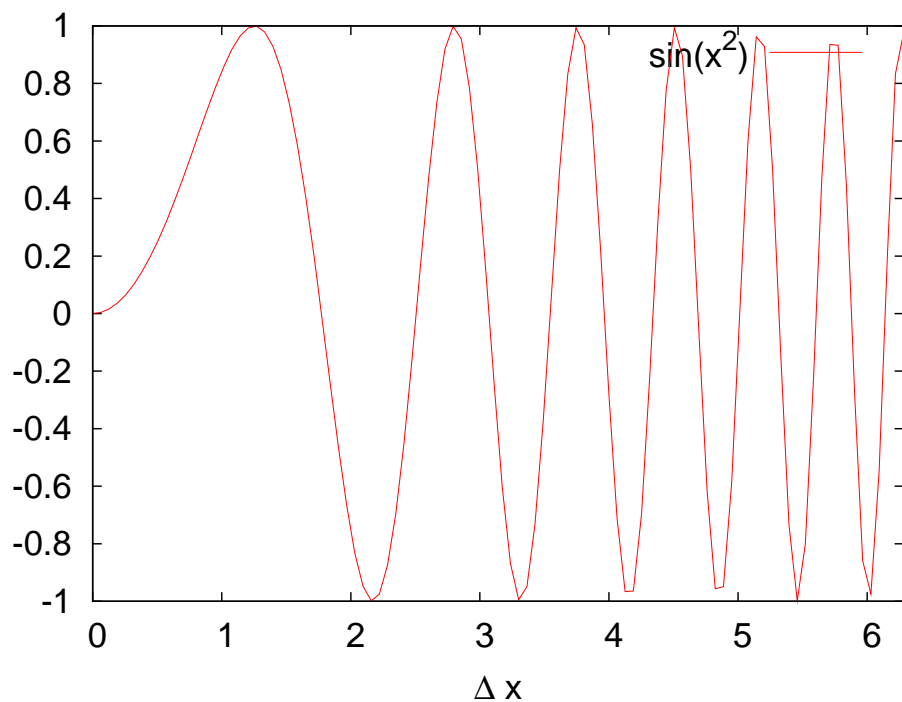


Figure 2.2: Sample figure drawn by Gnuplot

Table 2.1: Sample Table

Row 1	Row 2	Row 3
1	2	3
4	5	6
7	8	9

2.2 How to Deal with Errors

if you refer so many figures and tables, you may see the error message below.

! LaTeX Error: Too many unprocessed floats.

In that case, please insert `\clearpage` appropriately.

References

- [1] K. Katsuki, M. Kotani, K. Kobayashi, and H. Onodera, “A 90 nm LUT array for speed and yield enhancement by utilizing within-die delay variations”, *IEICE Transactions on Electronics*, Vol. 90, No. 4, pp. 699–707, (2007).
- [2] Y. Tosaka, R. Takasu, T. Uemura, H. Ehara, H. Matsuyama, S. Satoh, A. Kawai, and M. Hayashi, “Simultaneous Measurement of Soft Error Rate of 90 nm CMOS SRAM and Cosmic Ray Neutron Spectra at the Summit of Mauna Kea”, *Reliability Physics Symposium, 2008. IRPS 2008. IEEE International*, (2008), pp. 727 –728.
- [3] J. Choi, D. Tsukiyama, and J. Rivas, “Evaluation of a 900 V SiC MOSFET in a 13.56 MHz 2 kW resonant inverter for wireless power transfer”, *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, (2016), pp. 1–6.
- [4] Takao Hirasawa, “*Power Electronics*”, Kyoritsu Shuppan company limited, (1992).