バッファチェインにおける パルス幅縮小現象を利用した SETパルス幅測定回路

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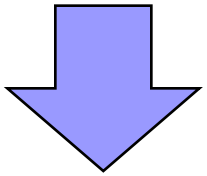
Purpose & Contributions

- Process scaling makes LSI more susceptible to soft errors
  - Both SEU and SET become dominant

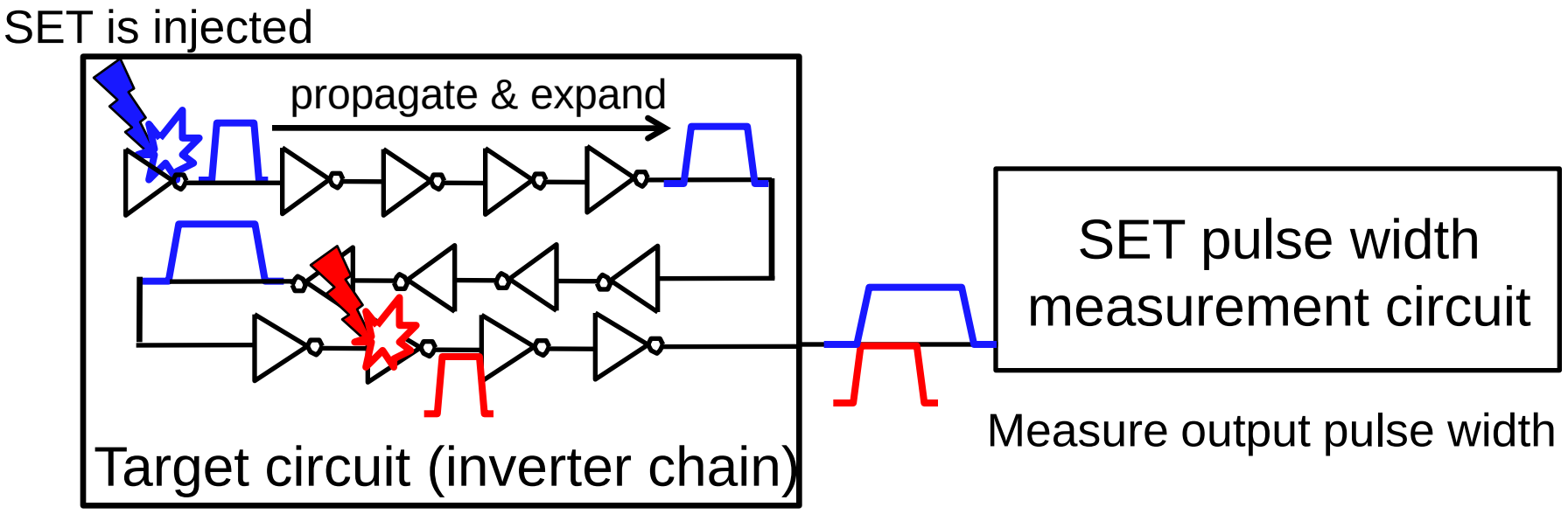


- Measure neutron-induced SET pulse width on a buffer chain
  - Propose an SET pulse width measurement circuit using propagation-induced pulse shrinking
  - SET pulse widths are exponentially-distributed
  - SETs over 350ps can be reduced by inserting tap-cell closely

Outline

- Purpose & Contributions
- Proposed Structure
- Experimental Setup
- Experimental Results
- Conclusions

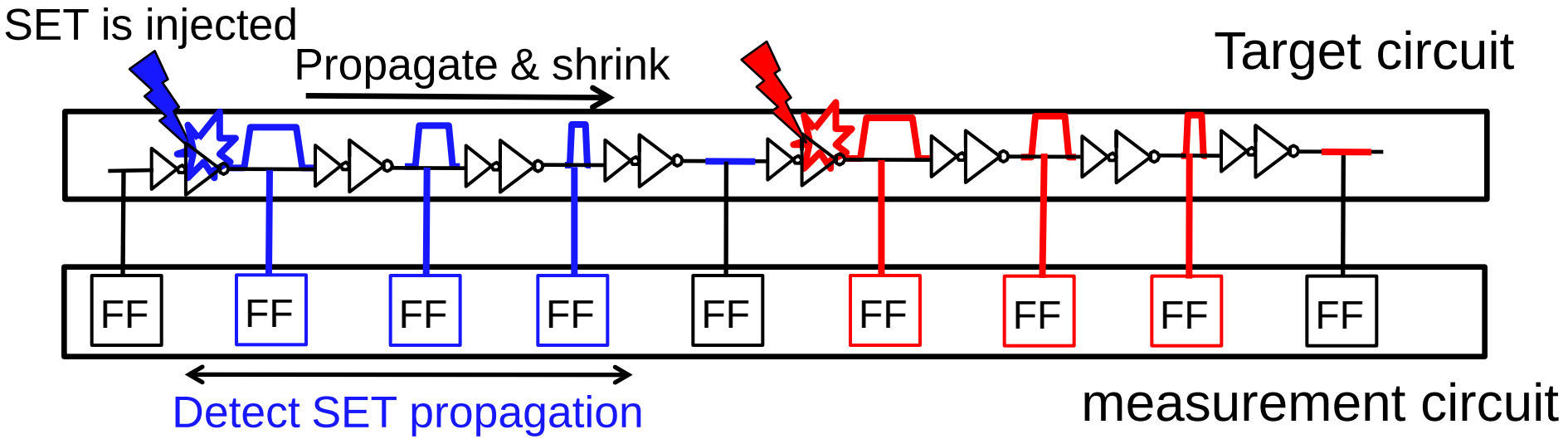
What's the Problem of Conv. Cir.?



- Output pulse width depends on where SET is injected
  - SET pulse width linearly changes as it propagates

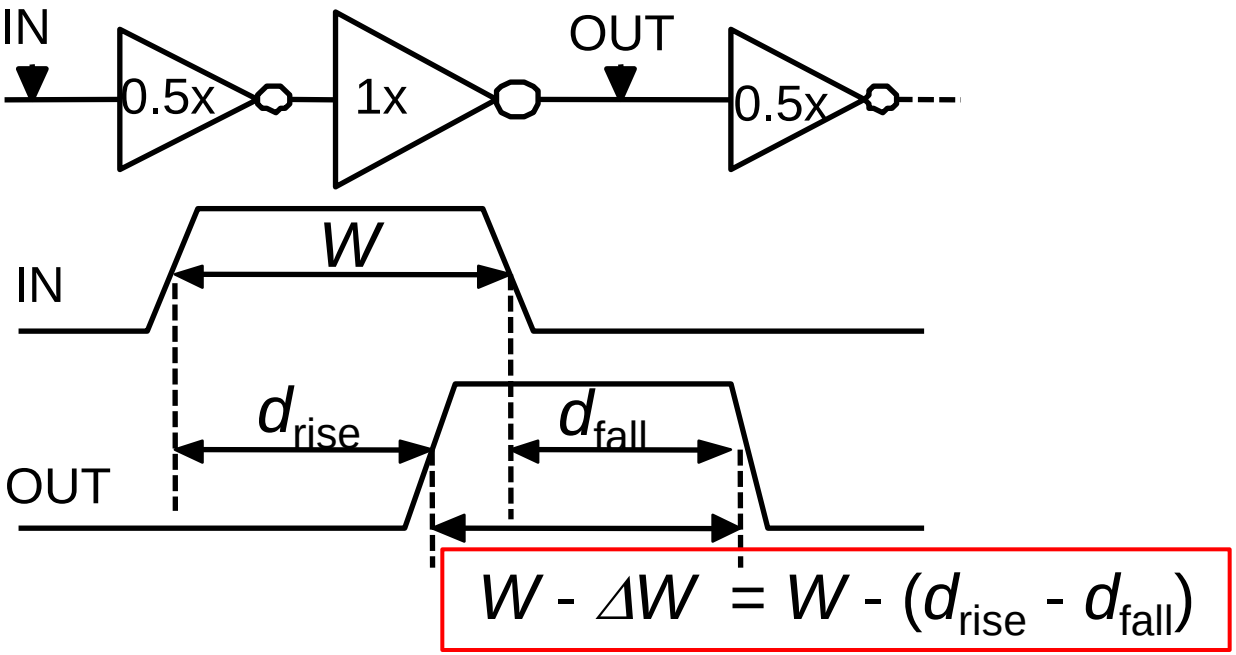
- SET pulse width cannot be measured accurately

Concept of Proposed Circuit



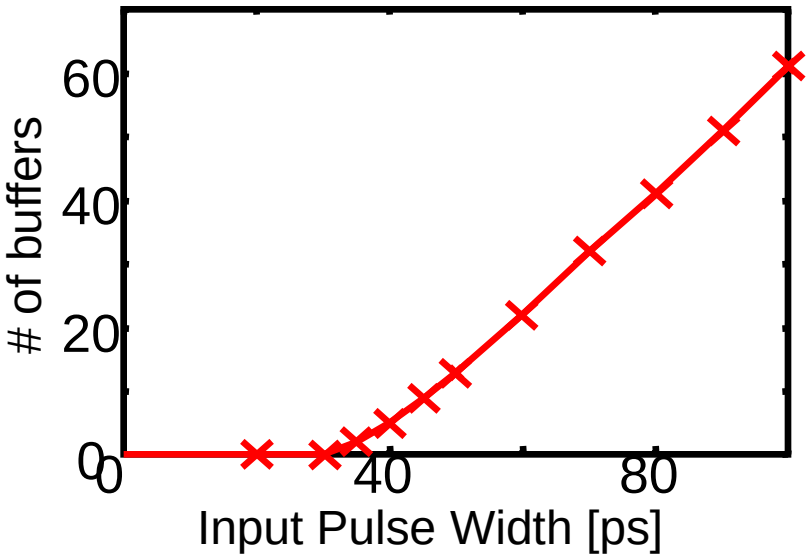
- Target circuit (buffer chain)
  - Linearly shrink SET pulse width as it propagates
- Measurement circuit (Flip-Flops)
  - Detect SET propagation of each buffer output
  - Measure SEUs and MCUs on Flip-Flops

Propagation-induced Pulse Shrinking on a buffer chain

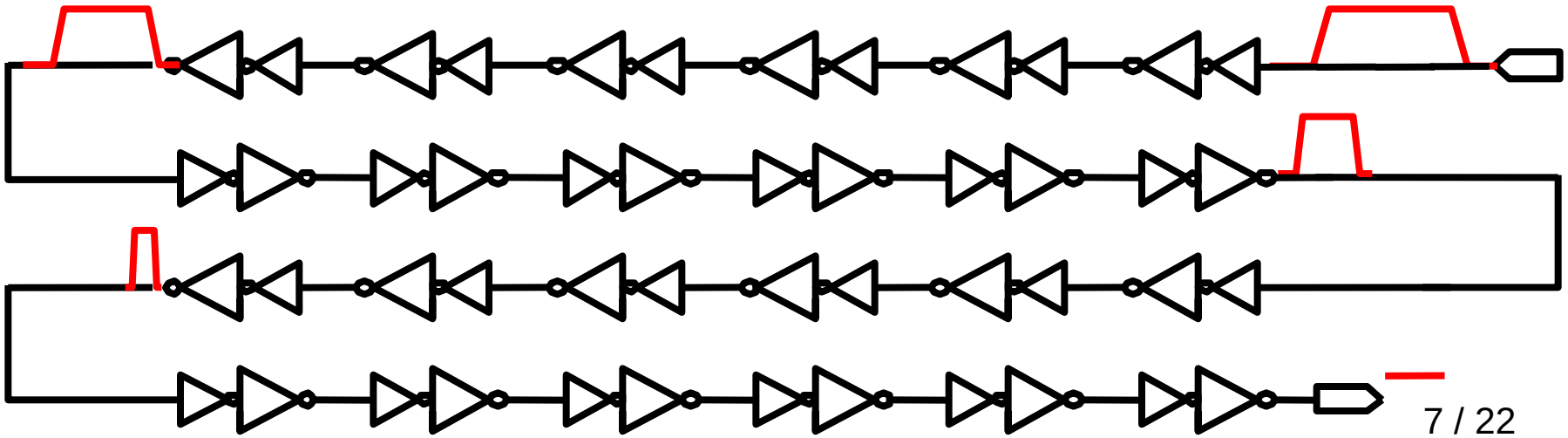


- Pulse shrinking, ΔW is caused by (d_{rise} - d_{fall})
  - d_{fall} / d_{rise} = fall / rise propagation delay of a buffer
- ΔW can be controlled by PMOS and NMOS sizes

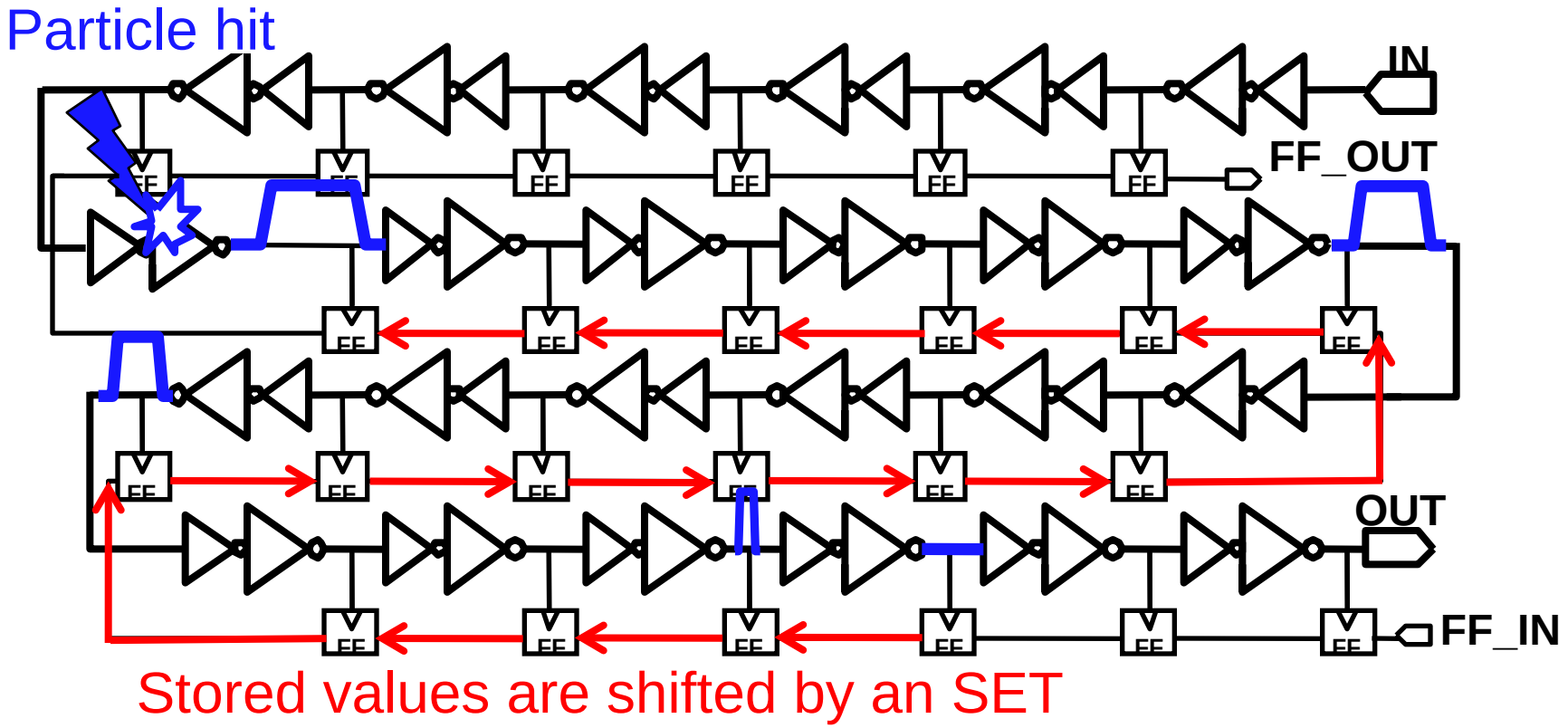
Simulation Results of Pulse Shrinking



- linearly shrinking up to 40ps
  - Can measure pulse width using pulse shrinking
  - Must measure # of buffers

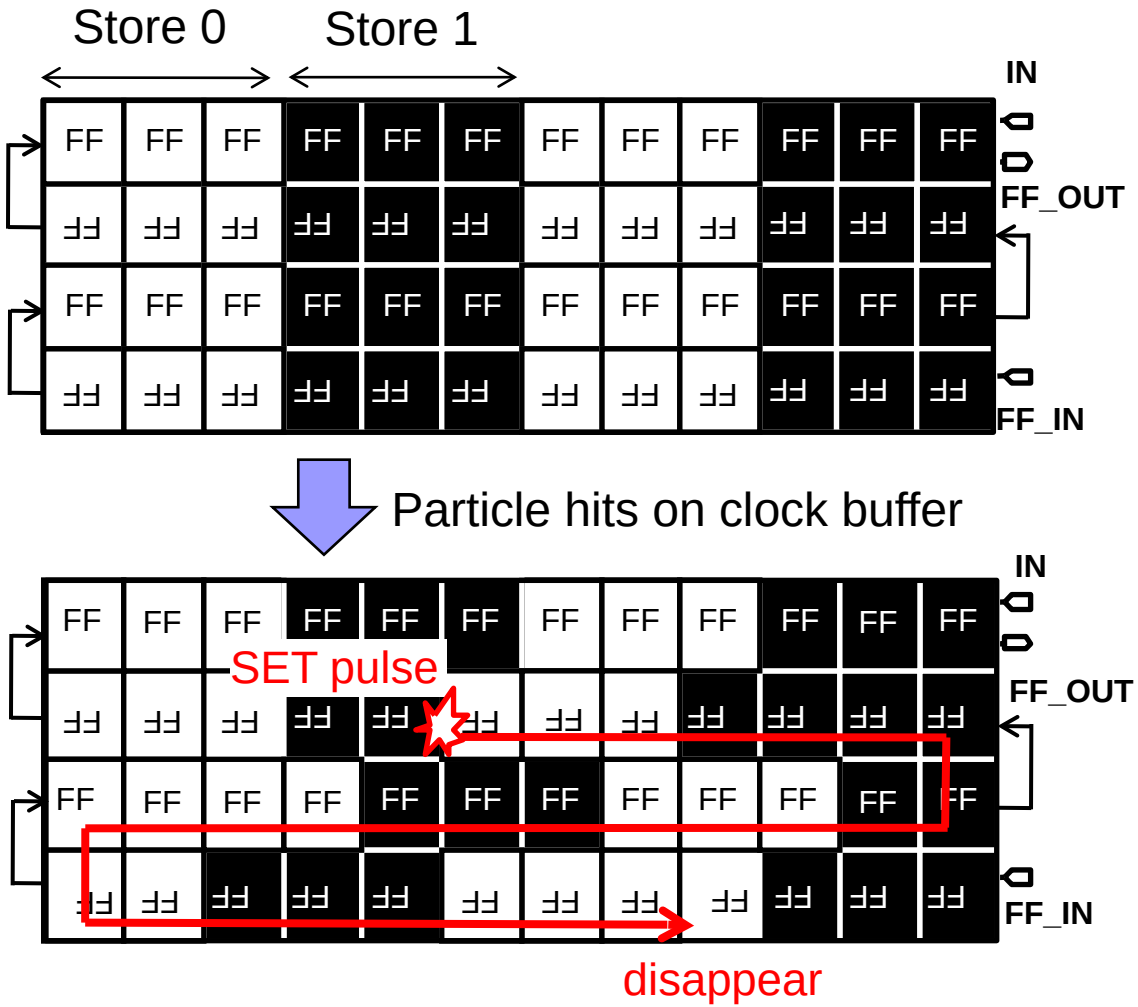


Proposed Circuit Structure



- Each buffer output is connected to a clock input of FF
  - FFs construct a shift register (buffer chain = clock tree)
  - # of buffers where SET propagates = # of shifted FFs

How to Measure # of buffers propagated by an SET pulse

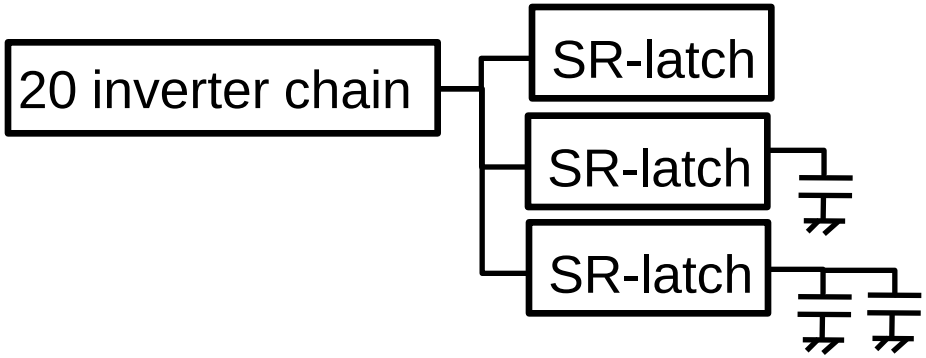


- All FFs are initialized to stripe pattern
- Measure number of shifted FFs
- Resolution depends on stripe pattern width

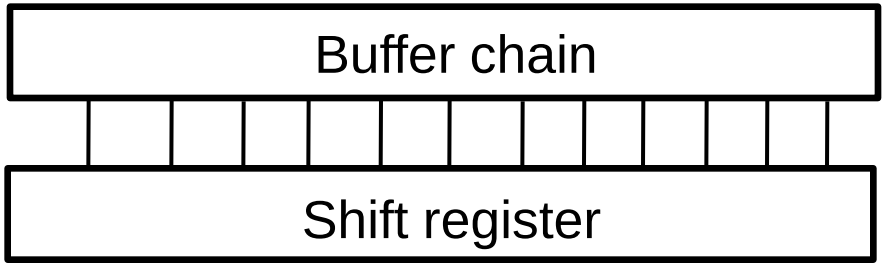
Comparison of Conventional and Proposed Circuits (1/2)

[5] Narasimham et. al., IRPS2008

[6] Nakamura et. at., IRPS2010



This work



Comparison of Conventional and Proposed Circuits (2/2)

	Narasimham[5]	Nakamura[6]	This work
Connection to target cir.	In series	In series	In parallel
accuracy	Inaccurate	Accurate	Accurate
Range	Average	Short	Long
Measurement method	Propagation delay	Min. pulse width	Pulse shrinking
Measurement of SEUs	No	No	Yes
Circuit size	Small	Large	Large

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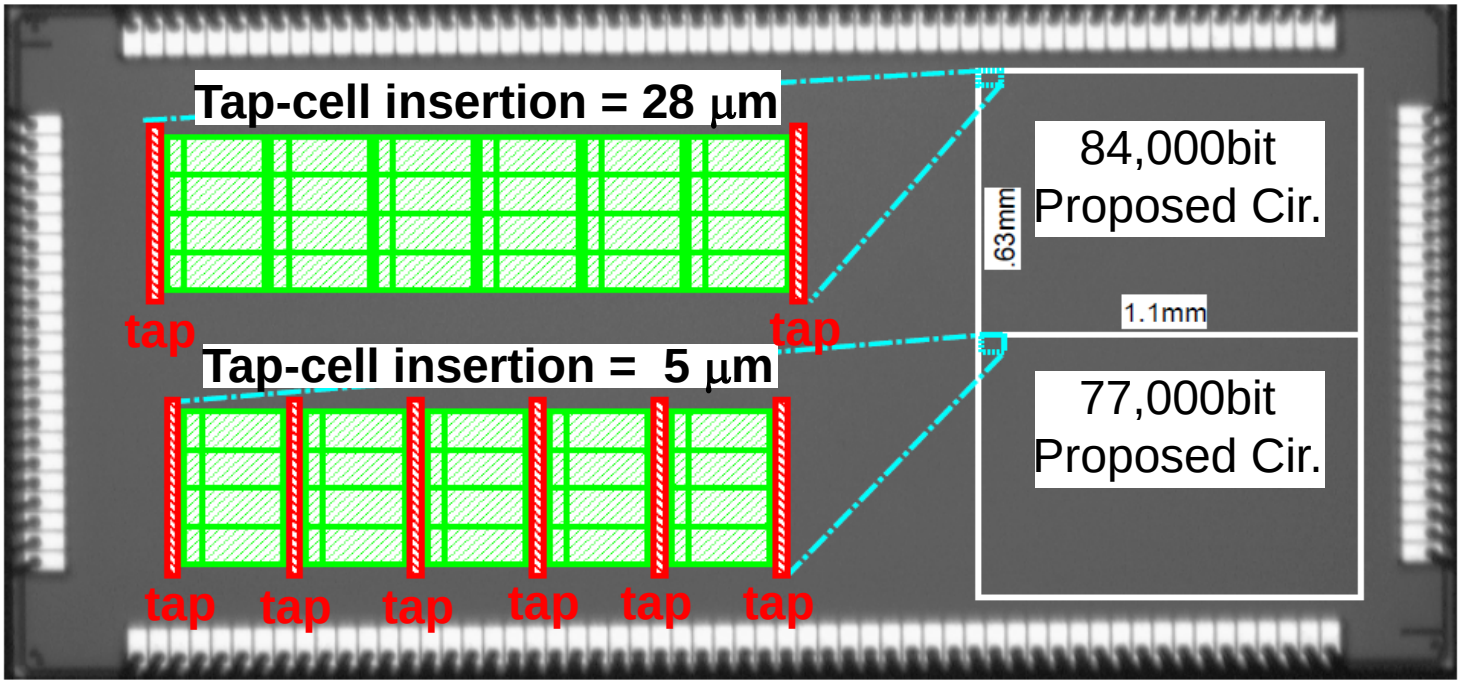
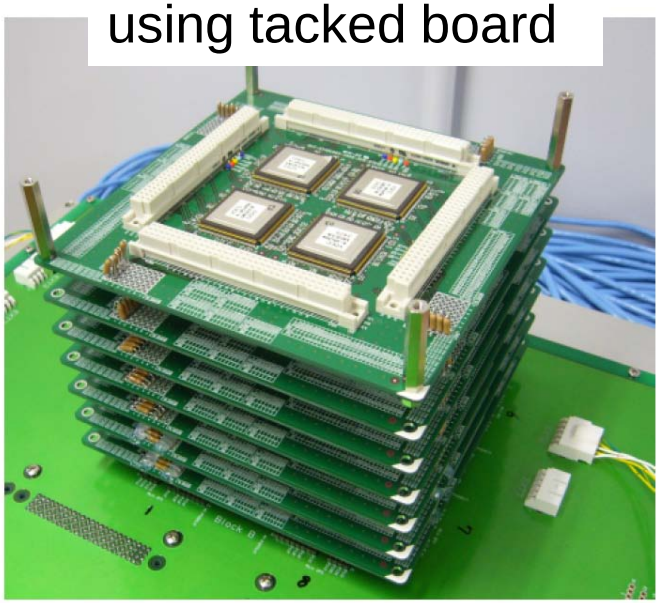
Chip Micrograph

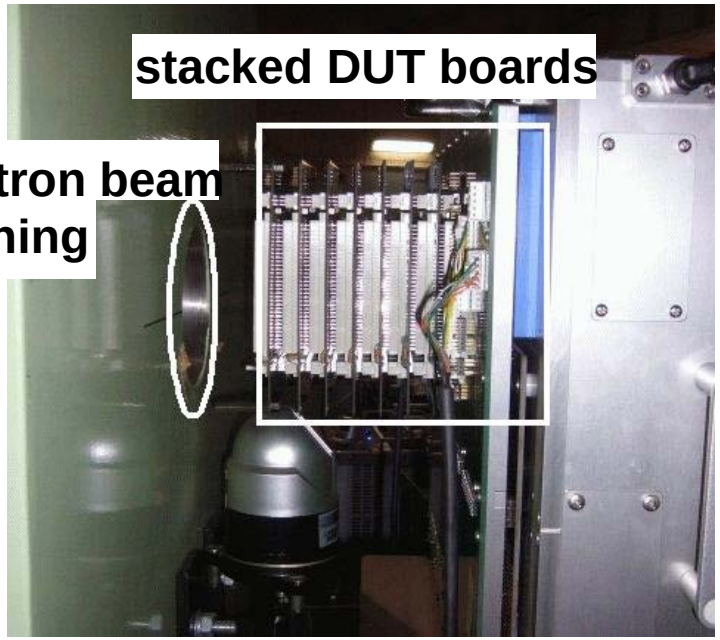
- 65nm bulk CMOS process on a 2 x 4 mm^2 die
  - Implement 161,000 bit shift register
- Tap-cell insertion :
  - Top 84,000 bit = 28 μm, Bottom 77,000 bit = 5 μm
  - Tap-cells stabilize well potential



Experimental Test Setup

Measured 18 DUTs using tacked board





- Accelerate at RCNP (Research Center for Nuclear Physics, Osaka University)
- Retrieve stored values every 5 minutes
- Initialize all FFs to 20bit stripe pattern
  - To measure MCUs (Multiple Cell Upset) simultaneously

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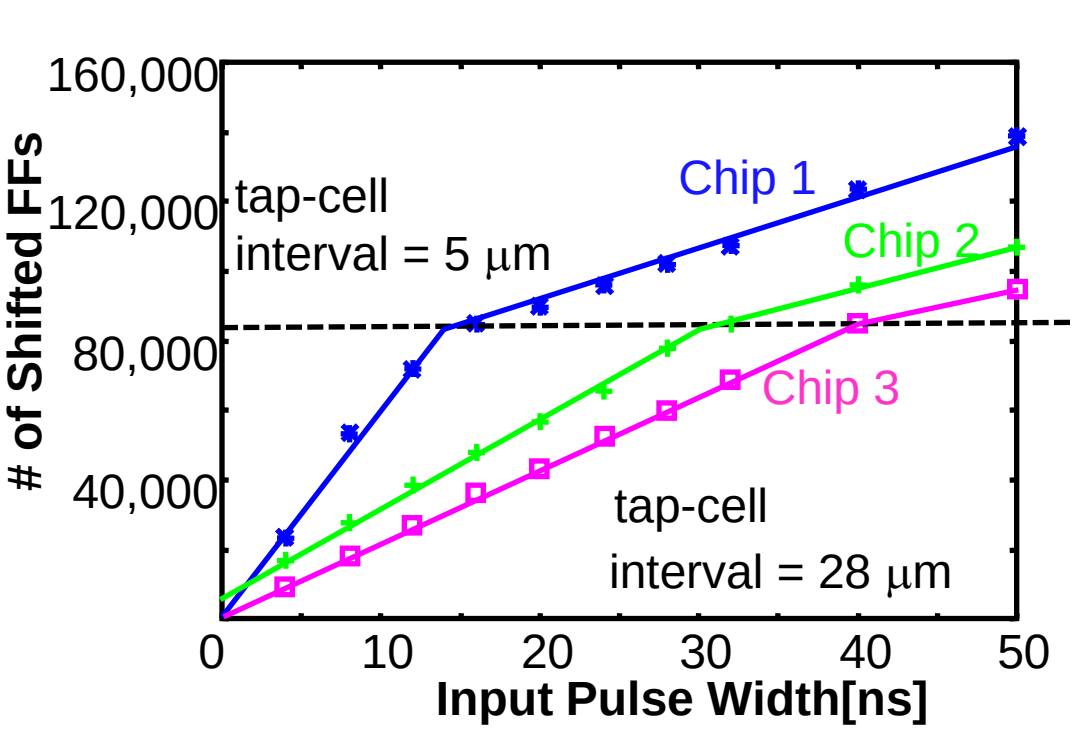
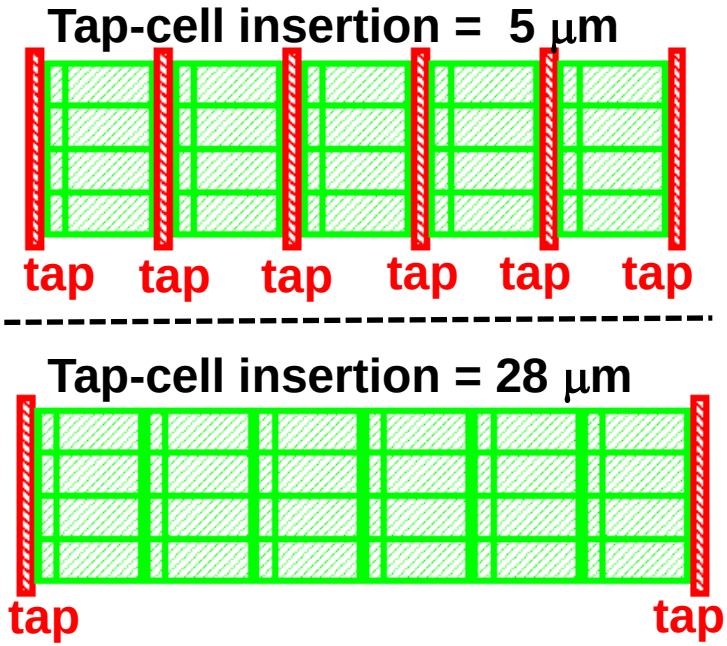
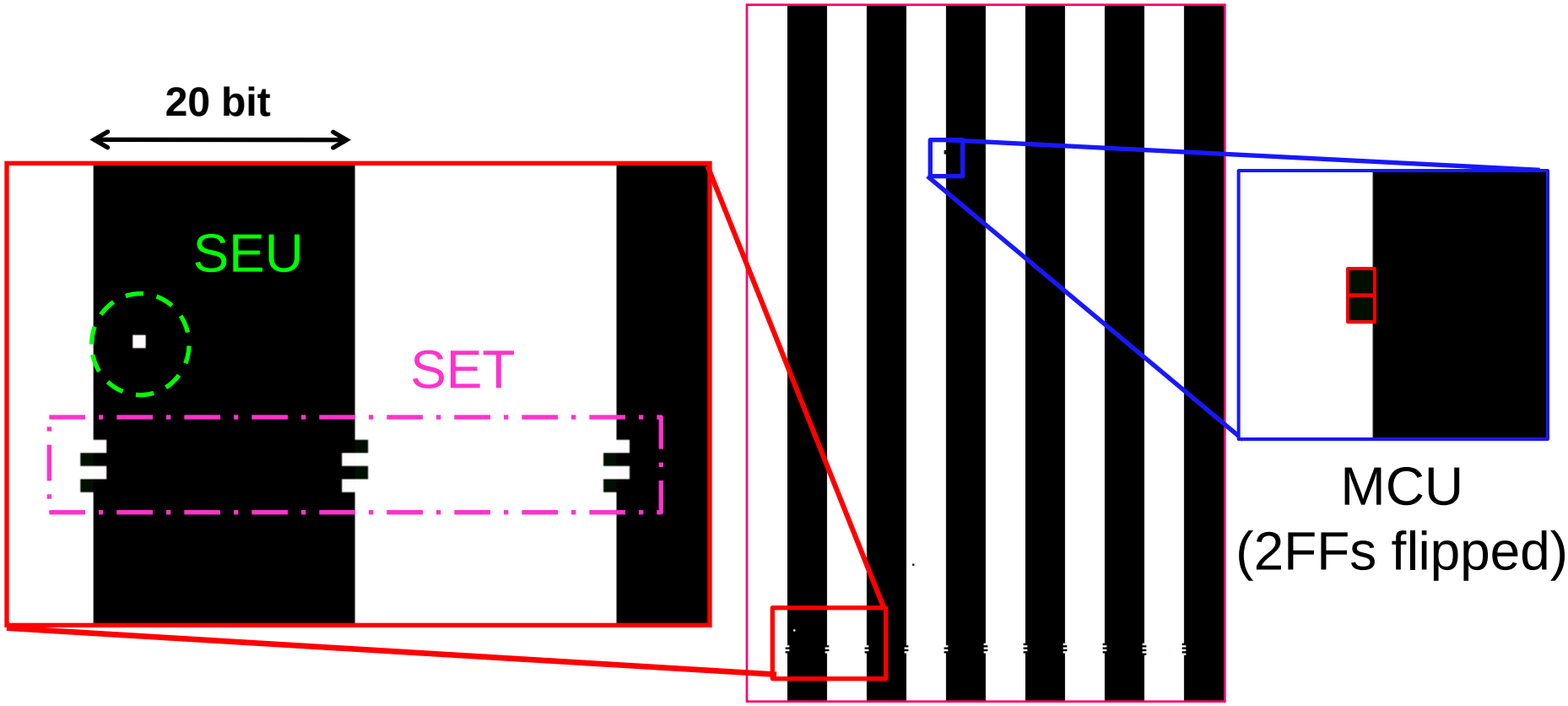
Calibration results





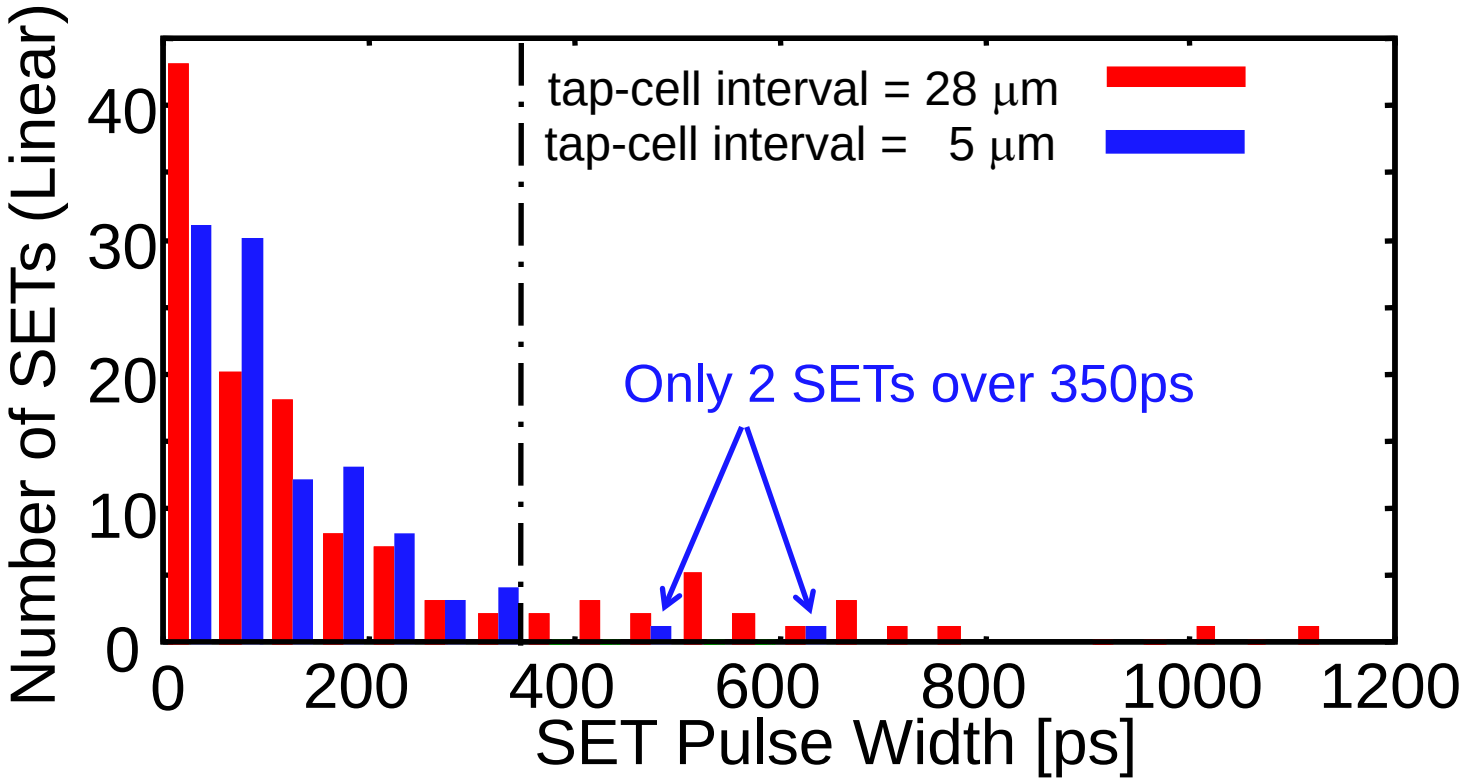
- Measure resolution (ΔW) by injected pulses
  - # of FFs linearly depends on input pulse width
- Different resolutions for each chip and tap-cell interval
  - Resolution : 0.16~1.0ps / buffer

Example of Measurement Results



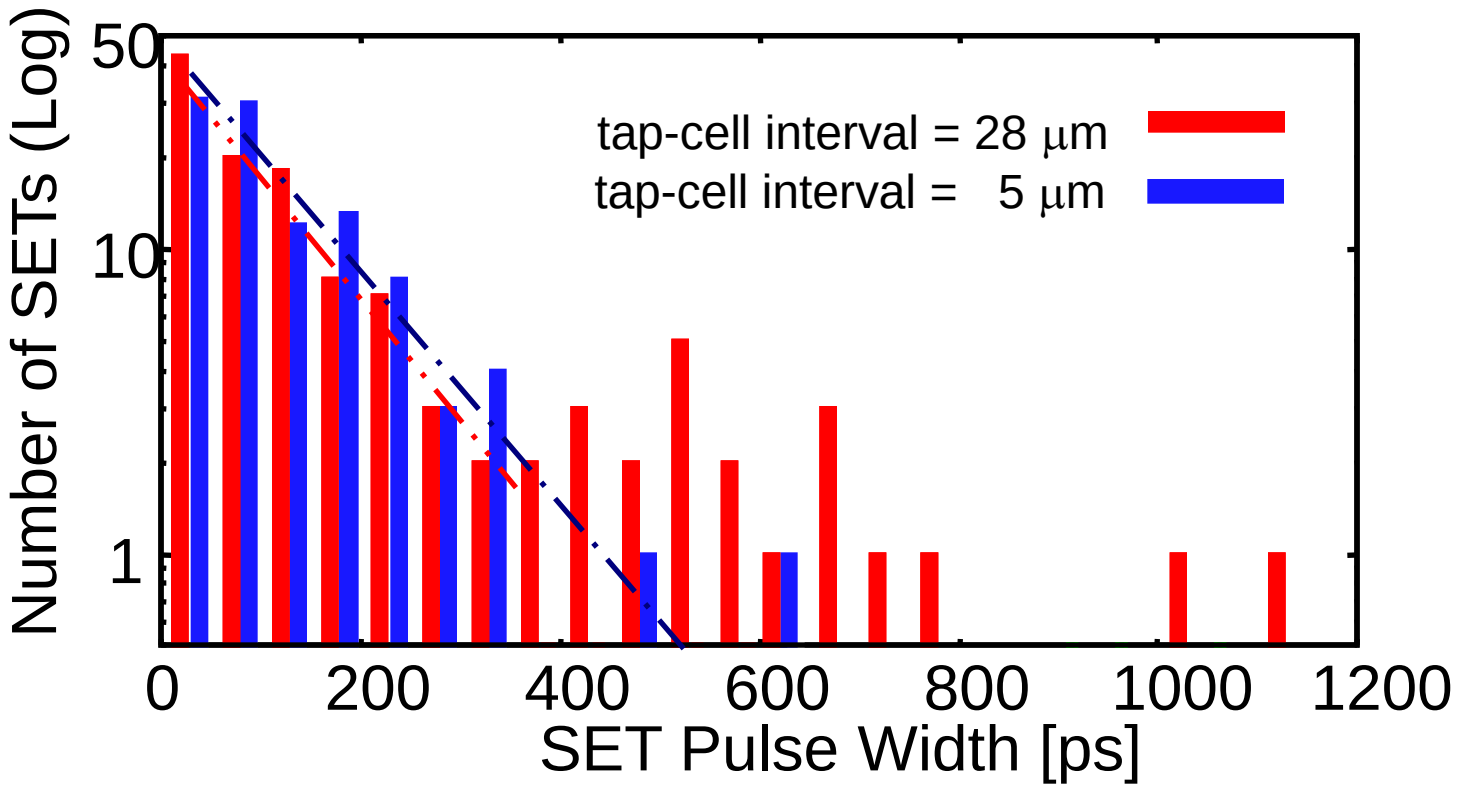
- SET pulse width, SEUs and MCU were measured using the proposed circuit

Distribution of SET pulse width (1/2)



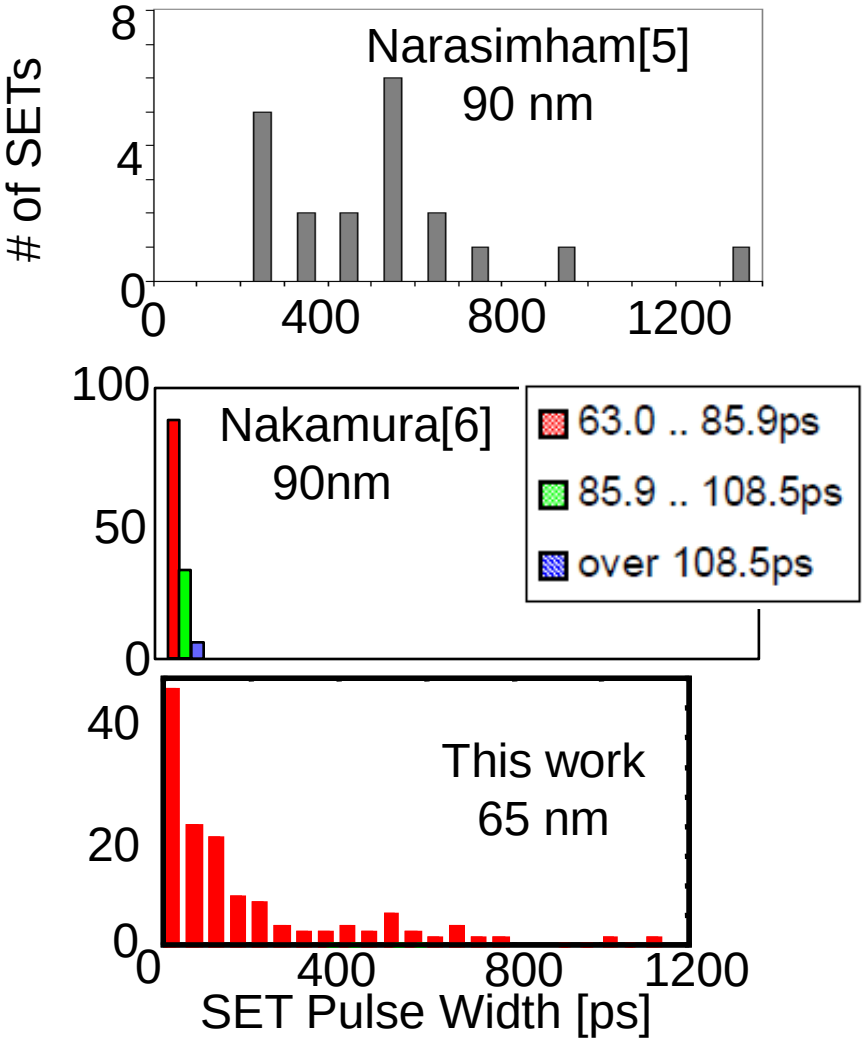
- Shorter SETs have higher probability
- SET pulse widths are reduced by inserting tap-cell
  - SETs over 350ps are reduced from 22(28μm) to 2(5μm)

Distribution of SET pulse width (2/2)



- SET pulse widths are exponentially-distributed
  - Excluding SETs over 350ps on 28 μm tap-cell interval
  - Parasitic bipolar effect prolongs the pulse width

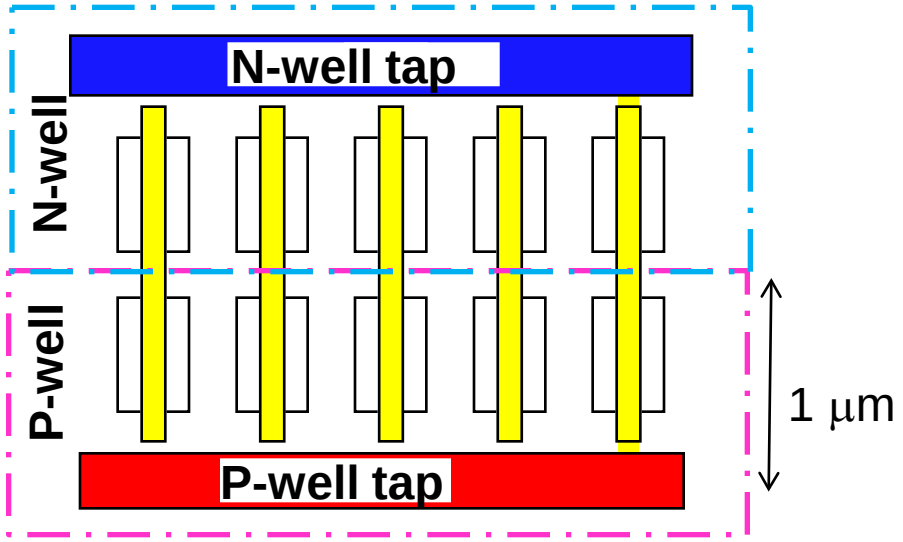
Comparison of Results (1/2)



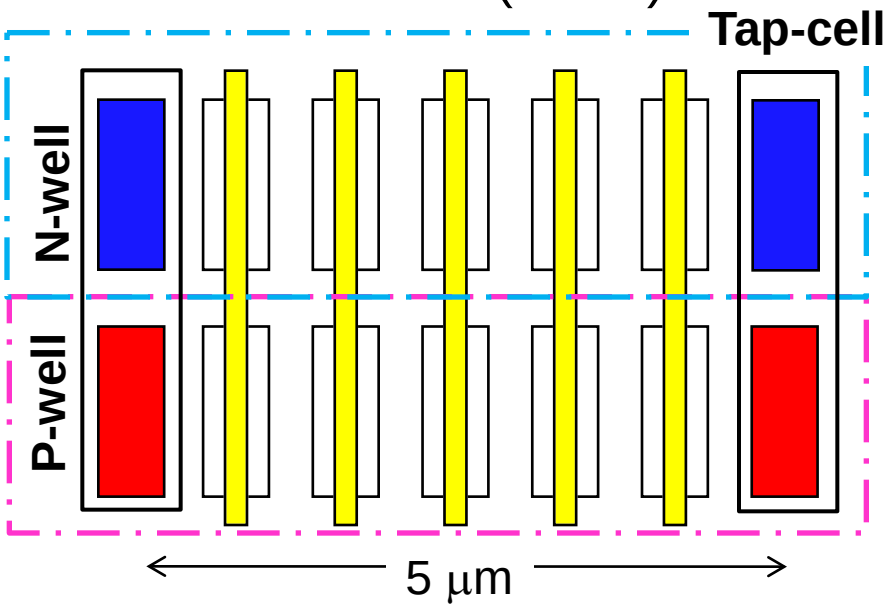
- Similar to Nakamura's results
  - Shorter SETs have higher rate
- Ratio of SETs over 100ps
  - Narasimham : 100%
  - Nakamura : 5~10%
  - This work : 40%(5μm), 50%(28μm)
- Nakamura's circuit has higher tap-cell density

Comparison of Results (2/2)

Nakamura's structure (90nm)



This work's structure (65nm)



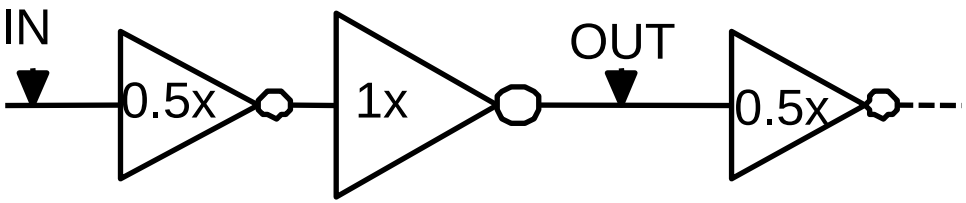
- Nakamura's structure has well-taps under VDD and GND metal layers
  - 2.5x higher density than our structure (5 μm)

K. Tanaka, H. Nakamura et. al., SISPAD2009

Conclusions

- Propose an SET pulse width measurement circuit using propagation-induced pulse shrinking
  - less affected by the propagation effect
  - No dependence on where an SET is injected
- Measured SET pulse width by neutron irradiation
  - Shorter SETs has higher probability
  - SET pulse widths are exponentially-distributed
  - SETs over 350ps are reduced to 9% by inserting tap-cell closely

Backup : Pulse Shrinking



- d_{fall} and d_{rise} are approximated as follows

$$d_{\mathrm{fall}} \approx k\left(\frac{C_{\mathrm{g}}}{0.5g_{\mathrm{mp}}}+\frac{0.5C_{\mathrm{g}}}{g_{\mathrm{mn}}}\right)$$

$$d_{\mathrm{rise}} \approx k\left(\frac{C_{\mathrm{g}}}{0.5g_{\mathrm{mn}}}+\frac{0.5C_{\mathrm{g}}}{g_{\mathrm{mp}}}\right)$$

  - g_{mp}, g_{mn} : transconductance of the 1x inverter
  - C_g : gate capacitance of the 1x inverter
- If $g_{mp} > g_{mn}$, pulse width is shrinking

$$\Delta W = d_{\mathrm{fall}} - d_{\mathrm{rise}} = \frac{3}{2}kC_{\mathrm{g}}\left(\frac{1}{g_{\mathrm{mp}}}-\frac{1}{g_{\mathrm{mn}}}\right)$$