超低電圧SRAMにおける中性子起因ソフトエラーの評価

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Introduction (1/2)

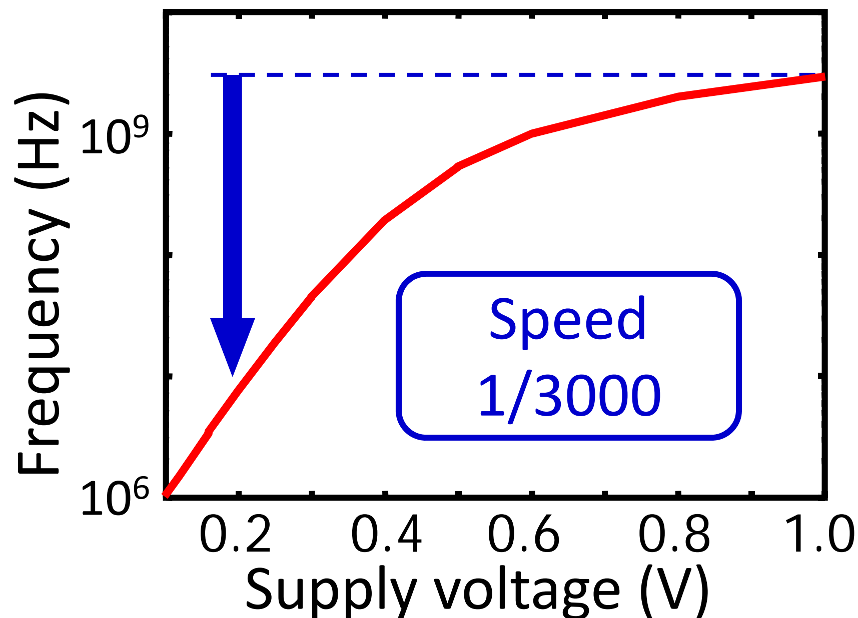
- Severely energy-constrained devices with low demands for speeds

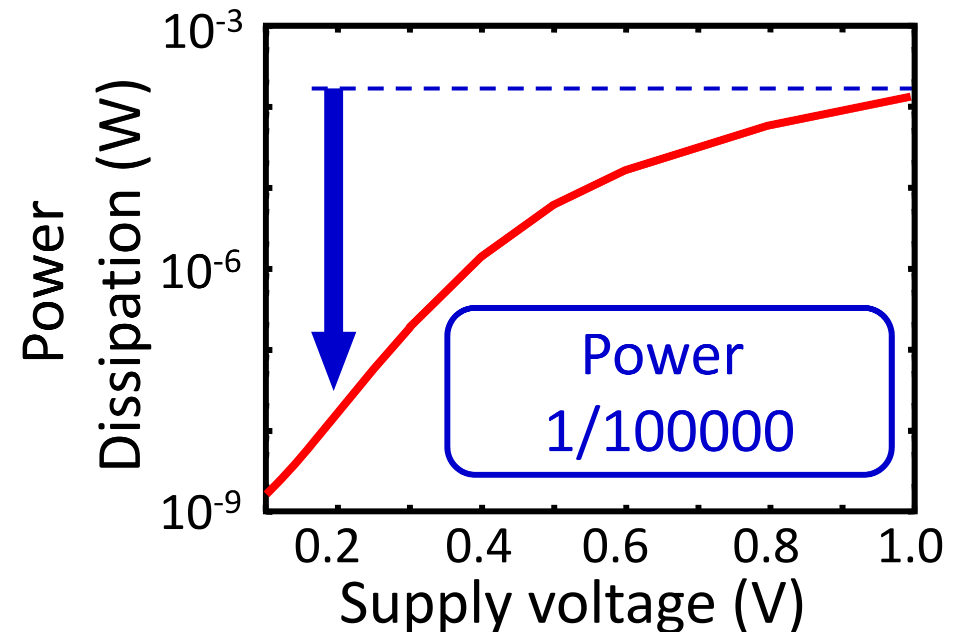
  (example)

  - Processors for sensor network
  - Medical applications

Introduction (2/2)

- Subthreshold circuits
  - Operate at lower supply voltage than threshold voltage
    for example, at VDD=0.3V
  - **Slow speed yet ultra-low power**

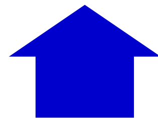




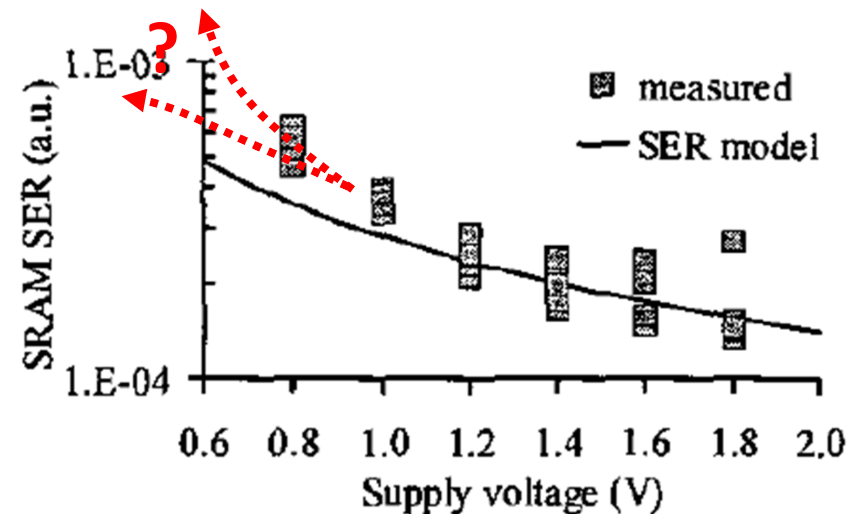
* Simulation of 17-stage ring oscillator (90nm process)

Motivation

- Soft error immunity of subthreshold circuits has become a concern.
  - Energy required to cause upsets decreases as supply voltage is lowered.
    - SRAM SER increases by 18% for every 10% reduction in VDD[1].

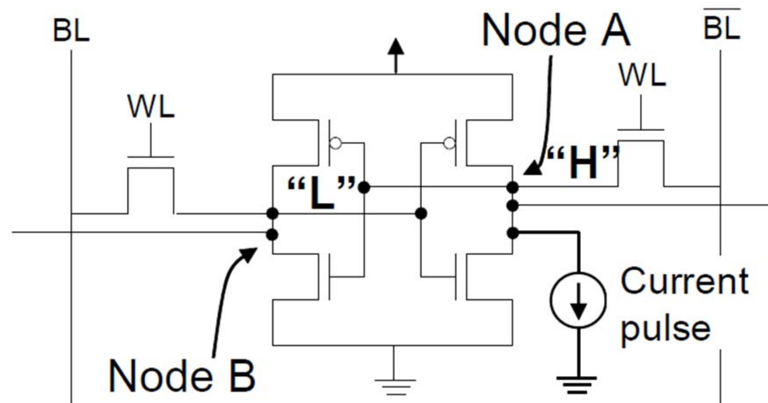


SRAM SER in subthreshold region has not been measured.

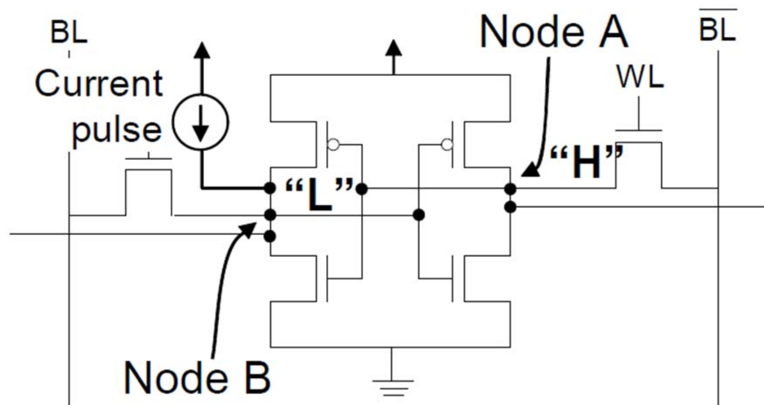


[1] P. Hazucha, et al., "Neutron Soft Error Rate Measurements in a 90-nm CMOS Process and Scaling Trends in SRAM from 0.25-μm to 90-nm Generation," *IEDM*, 2003.

Critical charge evaluation

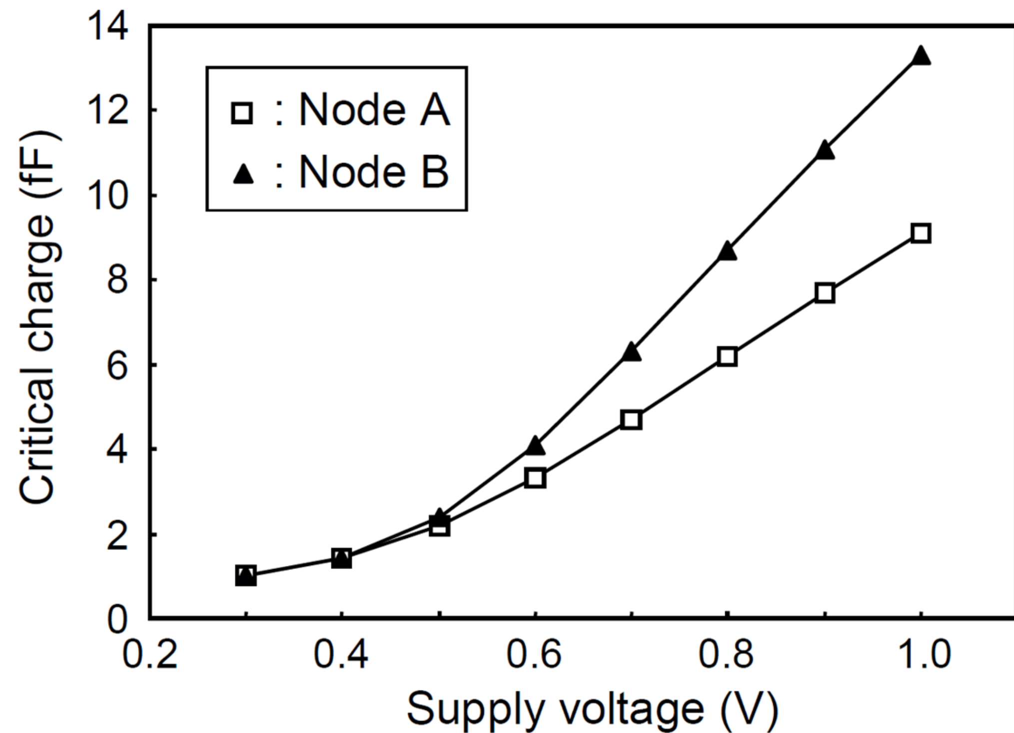


(a) strike on "Node A"



(b) strike on "Node B"

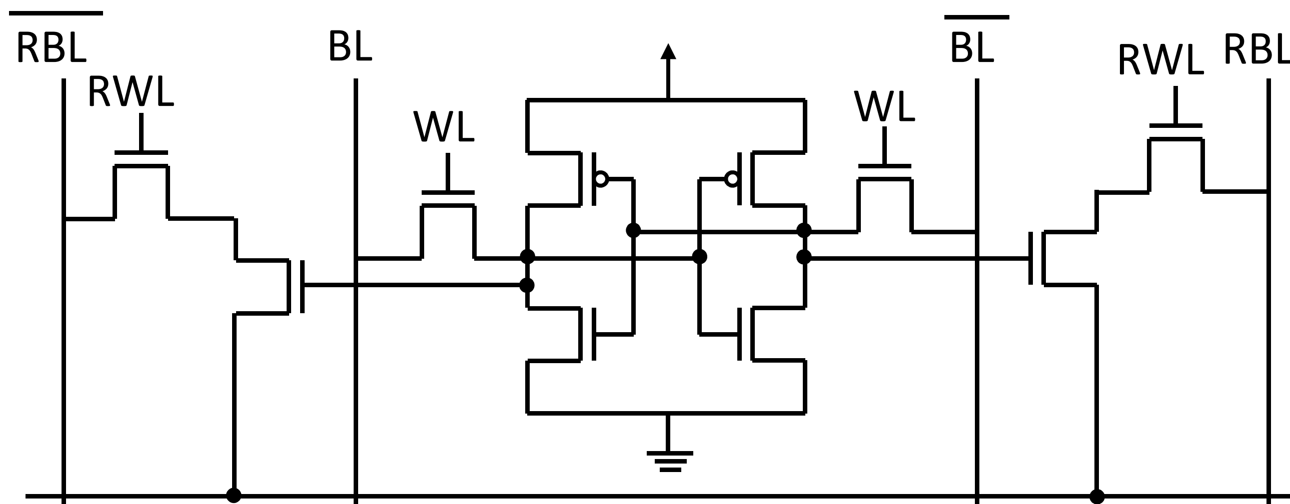
- Simulated w/ 2-exp current model in 65nm



Structure of Memory Cell

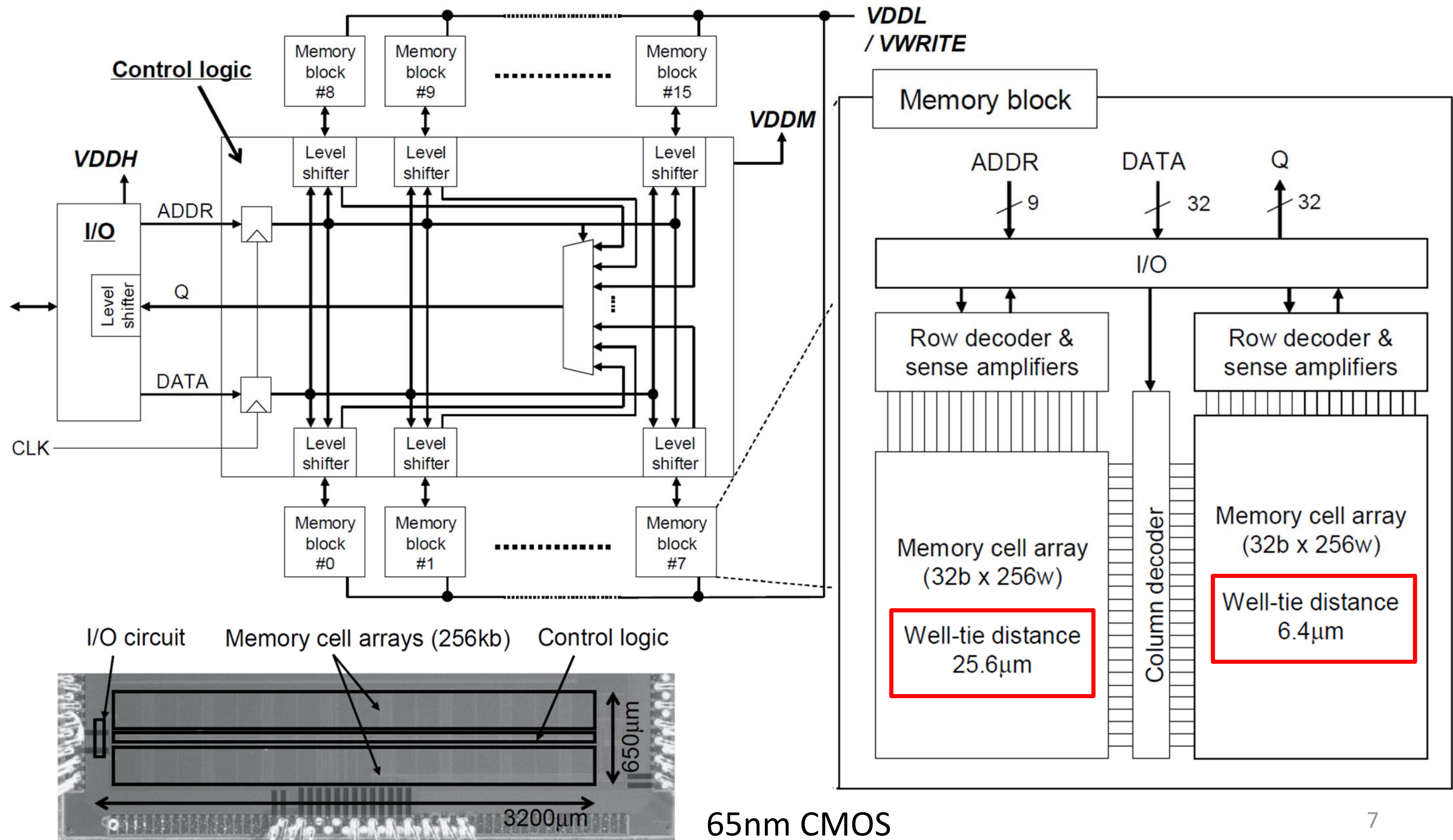
- Subthreshold SRAM
  - Traditional 6T SRAM does not function in subthreshold region due to weak writability and read instability.
  - Solutions **to add read port** have been proposed.

  → use 10T memory cell based on 8T memory cell [2]



[2] N. Verma, et al., "A 65nm 8T sub-Vt SRAM employing sense-amplifier redundancy," *ISSCC*, 2007.

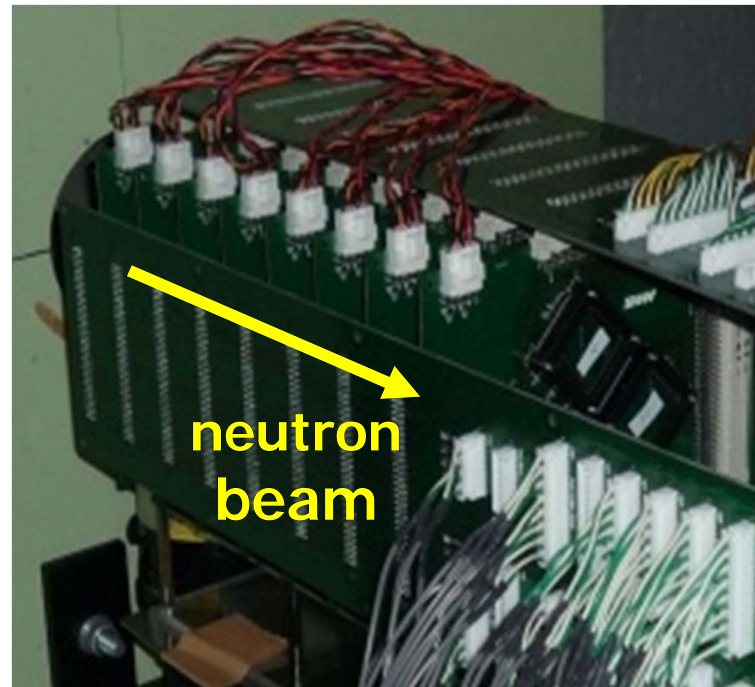
Test chip structure



65nm CMOS

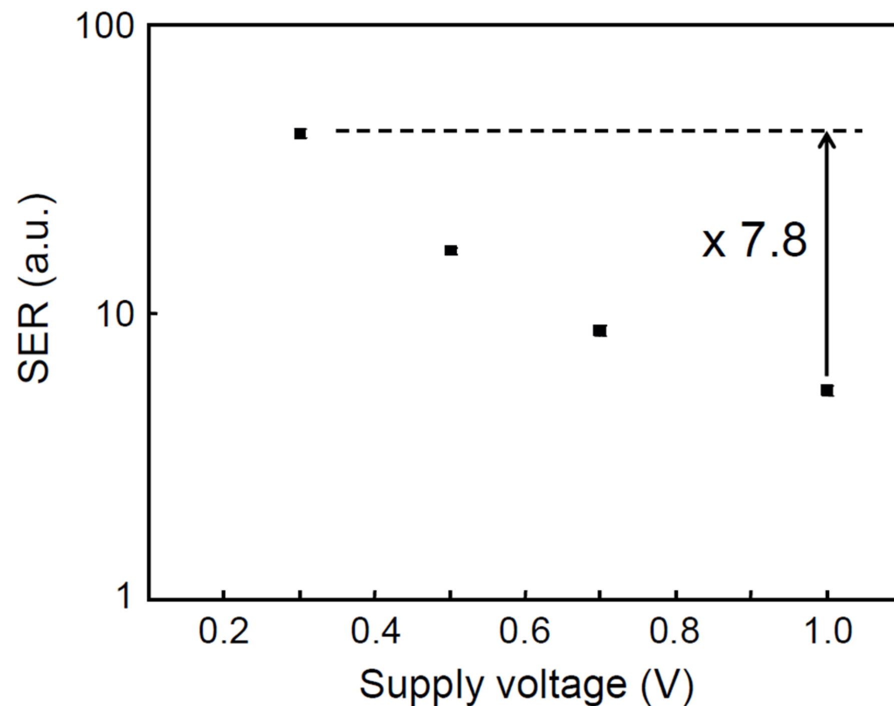
Setup for neutron radiation

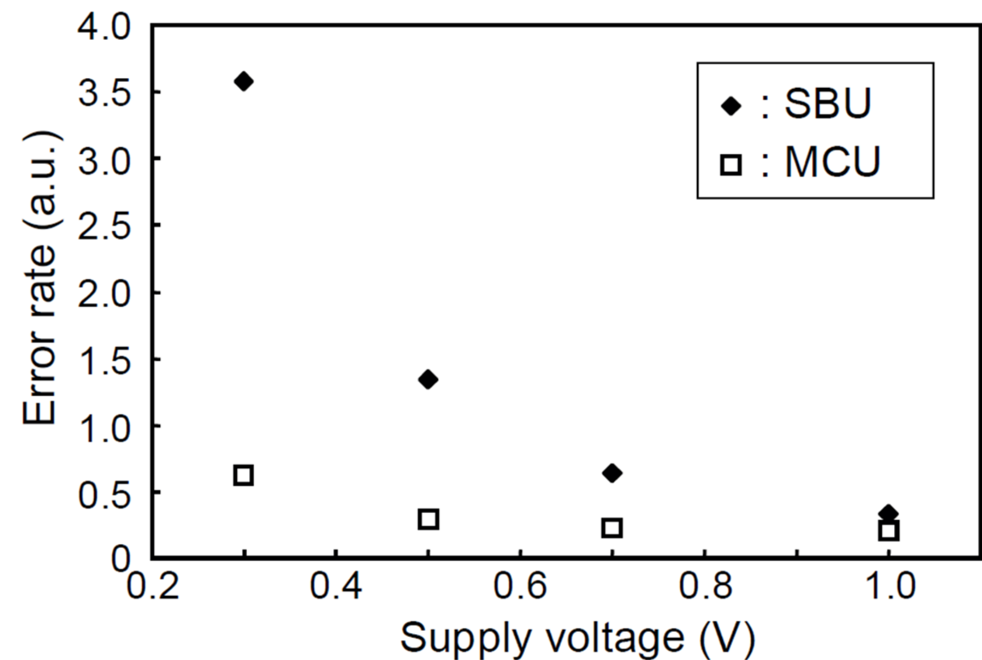
- Neutron radiation test was performed at RCNP
  - Flux of wide spectrum neutron beam is $2.41 \times 10^{9} cm^{-2} h^{-1}$
  - 7.75 Mb in total included in 31 chips were read every 60 secs.



VDD dependency of SBU and MCU

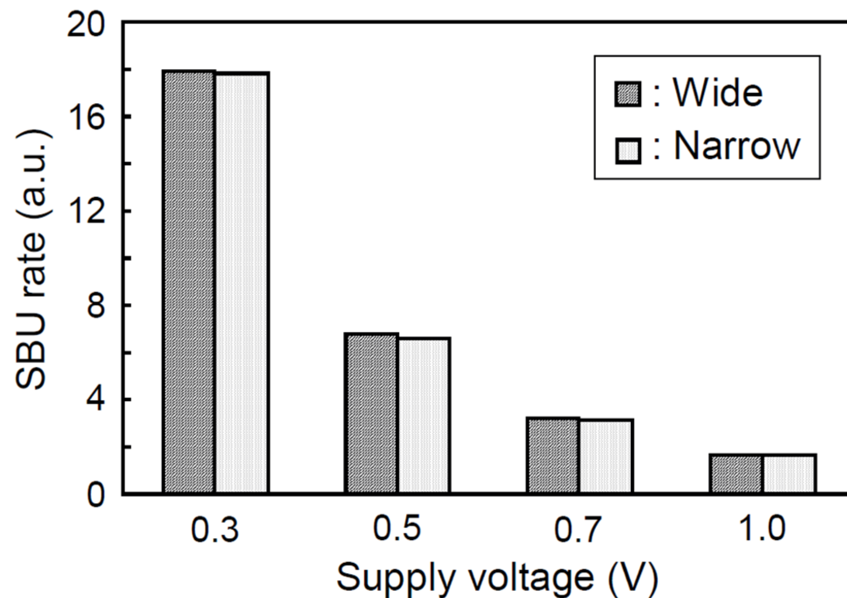
- Compared to 1.0V, SER at 0.3V is 7.8x higher
- Both SBU and MCU increase as Vdd decreases
  - SBU more drastically

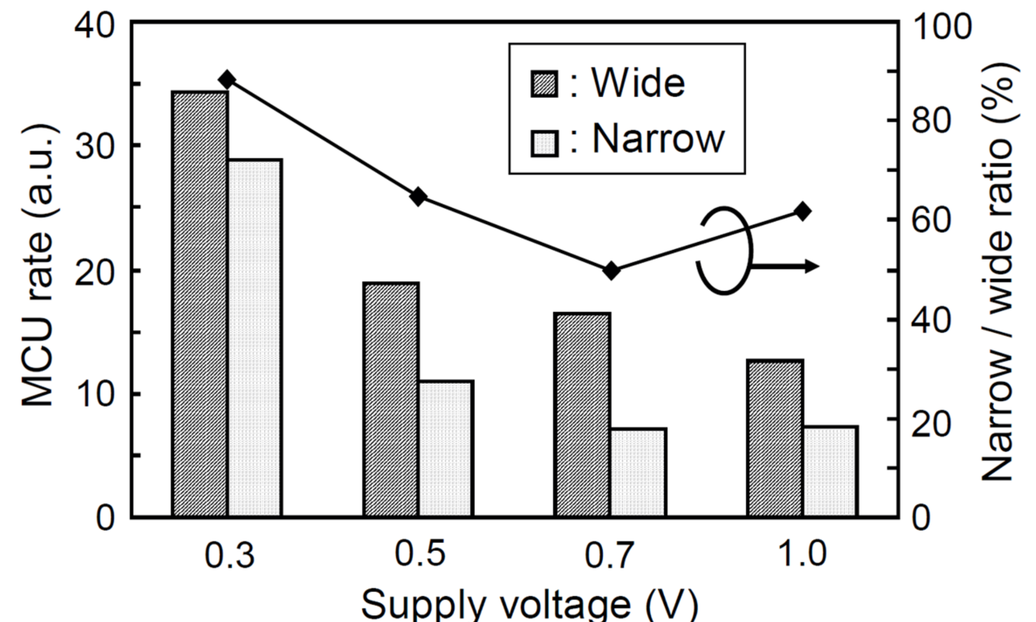




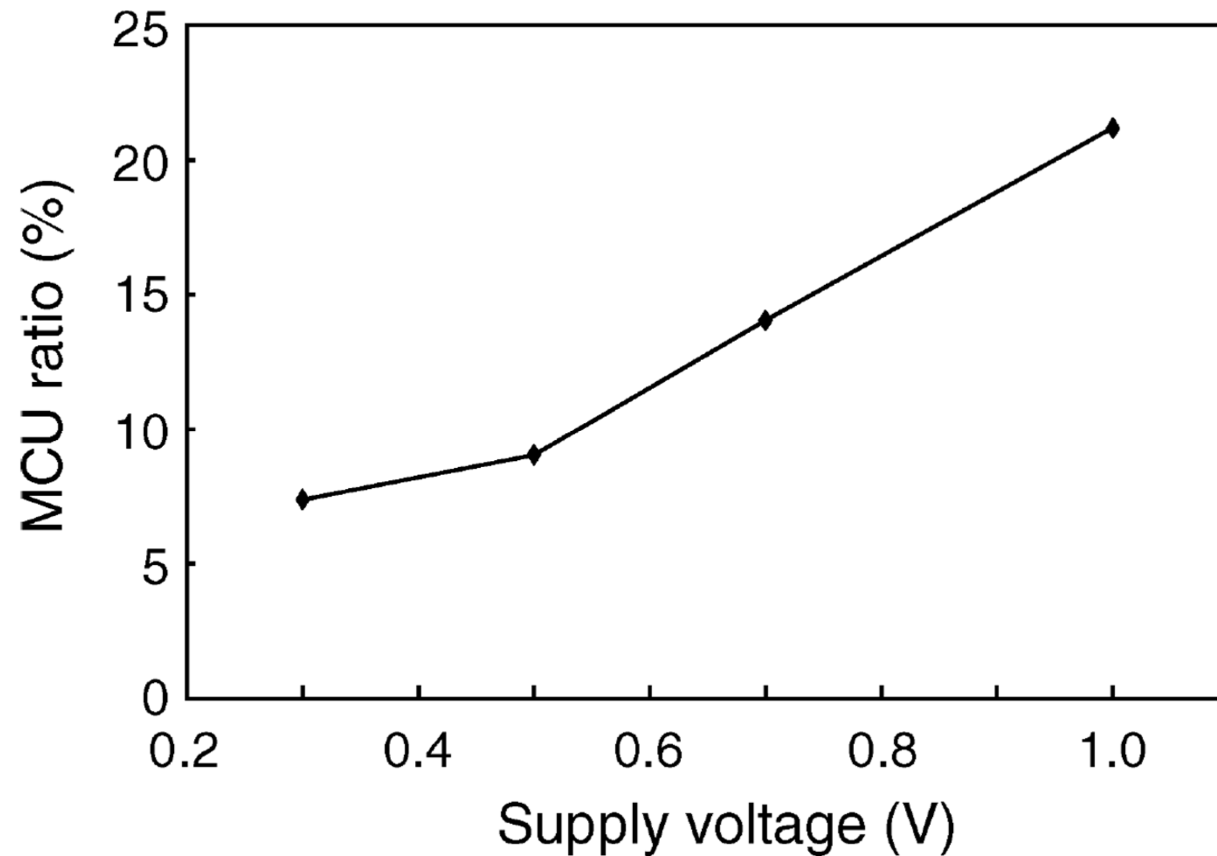
Dependency on well tap distance

- SBU is less independent on well tap distance
- MCU at high voltage is strongly dependent
  - Bipolar effect mainly induces MCU.
- MCU at low voltage is weakly dependent
  - Charge-sharing causes MCU.



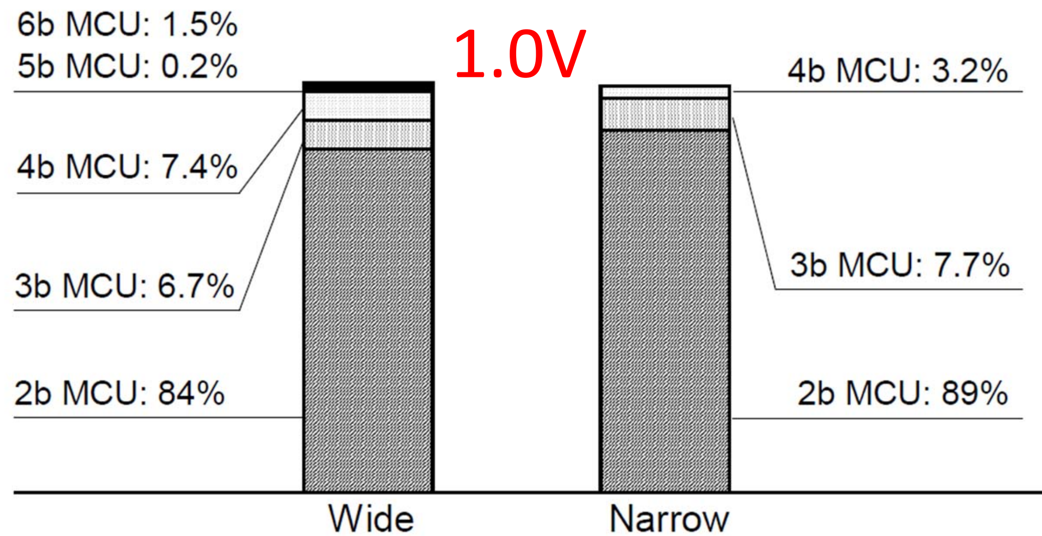


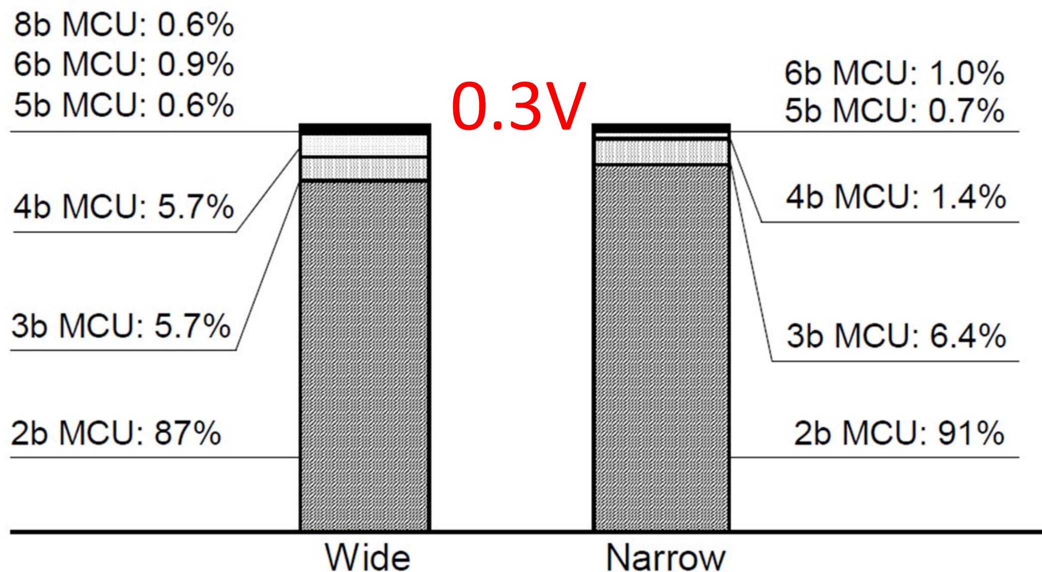
MCU ratio to total upsets



MCU ratio becomes smaller as supply voltage decreases due to dramatic increase of SEU.

#bits distribution of MCU





MCU with large bits happens at low voltage.

Conclusion

- SER at 0.3V is 8x higher than that at 1.0V for both alpha and neutron in 65nm subthreshold SRAM.
- MCU with large-bit upsets more likely happen at low voltage due to neutron.

超低電圧SRAMのソフトエラー 発表文献

- H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, ``Neutron-Induced Soft Errors and Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM,'' *IEEE Transactions on Nuclear Science*, vol. 58, no. 4, pp. 2097--2102, August 2011.
- H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, ``Alpha-Particle-Induced Soft Errors and Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM,'' *Proceedings of International Reliability Physics Symposium (IRPS)*, pp. 213--217, May 2010.